IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC., Plaintiff, v. FREESCALE SEMICONDUCTOR, INC., Defendant.	)	C.A. No. 06-788 (JJF)

FREESCALE'S ANSWERING CLAIM CONSTRUCTION BRIEF

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Dated: November 20, 2007

TABLE OF CONTENTS

TABLE OF AUTHORITIES

STATUTES

INTRODUCTION

The parties have taken markedly different approaches to construing the claim terms of the Fortin and Chan patents. As required by the Federal Circuit, Freescale looks to the evidence of what the inventors intended, as reflected in the intrinsic evidence (the patent claims, the patent specification and the file histories – i.e., the inventors' own words in describing their inventions and in distinguishing those inventions from the prior art). ProMOS, by contrast, often relies on unsupported attorney argument and rhetoric rather than evidence, and when it relies on evidence at all, ProMOS largely ignores the inventors' words, instead resorting blindly to dictionary definitions. As demonstrated in its opening brief and below, Freescale's approach is the correct one and its constructions should be adopted.

Before turning to the substantive arguments in detail, we note that ProMOS devotes considerable space in its opening brief to ad hominem attacks and the imputation of improper motives to Freescale. Yet what ProMOS's criticisms come down to is that Freescale ultimately agreed that various initially-identified claim terms did not need to be construed and that Freescale tried to reduce further the burden of claim construction by attempting to reach compromise constructions with ProMOS. Plainly, ProMOS's attacks are unwarranted, as all Freescale did is meet its obligation to meet and confer. ProMOS's attacks also are ironic because it did not attempt to compromise on a single construction, and it added at the last minute a number of brand new constructions (for terms where ProMOS previously had refused to provide *any* constructions) and modified many other of its previously proposed constructions shortly before the parties' opening briefs were due. Unlike ProMOS, Freescale chose not to complain about these last-minute changes because complaining does not help the Court resolve the construction issues, and the parties were in fact able to manage each other's changes. But ProMOS's charges should be seen for what they are: the pot calling the kettle black.

THE FORTIN PATENT

Freescale's constructions rely on the well-established meanings of claim terms clearly adopted by Fortin, as shown by his description of his invention, his use of the terminology in the specification and claims, and his explicit statements about the meaning of the terms during prosecution to overcome the prior art. In contrast, ProMOS relies on portions of a single prior art reference cited in the Fortin patent, without regard to Fortin's limited purpose in citing it for certain examples, the understanding of those skilled in the art or Fortin's own expressions about his invention in the prosecution history. Freescale submits that only its approach comports with the law governing claim construction and is the approach the Court should adopt.

I. DEPOSITION TERMS (PVD, CVD, AND SPUTTERING)

The parties' dispute over the meaning of the deposition terms of the Fortin patent (PVD, CVD and sputtering) involves two aspects: (1) the affirmative characteristics that should be included in each of the definitions (and how clearly they should be stated); and (2) whether the inter-relationships of those terms should be made clear, and in particular, that PVD and CVD are mutually exclusive and that sputtering is a form of PVD.

A. The Fundamental Concepts of PVD and CVD

As Freescale's opening brief explained, three central concepts should be included in the definitions of PVD and CVD: (i) the building up of material (i.e., the notion of "deposition"); (ii) the involvement of vapor; and (iii) the mechanism of action (DI 85 at 4, 10). Freescale cited intrinsic evidence showing what Fortin meant by PVD and CVD (including these concepts), as well as references in the art confirming that Fortin's descriptions are consistent with the ordinary meanings of these terms (*id.* at 4, 7-8, 10-13). Freescale's proposed definitions essentially adopt Fortin's descriptions of these claim terms in the prosecution and their incorporation of those three concepts:

PHYSICAL VAPOR DEPOSITION		
Freescale's Definition	**Fortin's Description**	**ProMOS's Definition**
A process of building up material on a surface in which the material to be deposited is released from a source of the material into a vapor phase by one or more physical mechanisms. Chemical vapor deposition is not physical vapor deposition or a type of physical vapor deposition.	"[A] general term for a deposition process in which the material to be deposited is released from the source of the material largely by one or more physical mechanisms." "CVD is not PVD or a type of PVD." DI 86, Ex. H at 9	A process in which films are deposited atomically by means of fluxes of individual neutral or ionic species.
CHEMICAL VAPOR DEPOSITION		
Freescale's Definition	**Fortin's Description**	**ProMOS's Definition**
A process of building up material on a surface in which a vapor formed with one or more chemical species that contain the material to be deposited, or components of the material to be deposited, undergoes suitable chemical reaction that enables the material being deposited to be released from the starting chemical species and accumulate on the deposition surface. Chemical vapor deposition is not physical vapor deposition or a type of physical vapor deposition.	"[A] deposition process in which a vapor formed with one or more chemical species that contain the material to be deposited, or components of the material to be deposited, undergoes suitable chemical reaction that enables the material being deposited to be released from the starting chemical species and accumulate on the deposition surface." "CVD is not PVD or a type of PVD." DI 86, Ex. H at 9	A process in which films are precipitated from the gas phase by a chemical reaction.

ProMOS's definitions simply ignore the inventor's own descriptions of what his claim terms encompass, and ProMOS's brief does not attempt to support its definitions from that standpoint or from what is generally understood in the art. Instead, ProMOS would support its definitions by quoting a reference cited in the Fortin specification, a handbook edited by Nishi (DI 84 at 35). Specifically, ProMOS argues that, "[t]he specification expressly states that the invention 'is applicable to TiN deposited by physical vapor deposition techniques' and by incorporating by reference the chapter of the handbook that related to PVD (pages 395-413) the

inventor left no room for doubt as to the proper definition of PVD" (DI 84 at 35). ProMOS does not otherwise rely on any statements from the intrinsic record about PVD or CVD.

ProMOS's argument that the inventor was relying on a chapter in the Nishi Handbook for definitions of PVD and CVD, and indeed that he "left no room for doubt," fails to closely analyze the patent and the limited propositions for which Fortin cited Nishi. The patent cites it in three places: (1) early in the Background section for the proposition that TiN is a barrier layer to the tungsten layer (1:17-24); (2) later as background for the fact that sputtering is "less complex and costly" than CVD for deposition of TiN (1:42-44); and (3) at the end of the specification (after describing the preferred embodiment) when elaborating on additional embodiments (4:49-56). The first citation is not addressed to deposition processes at all. The second is limited to Fortin's conclusion about relative cost and complexity of sputtering versus CVD, without characterizing either process technically.

Fortin's third citation, which is the one relied on by ProMOS, is made to support specific examples of "physical vapor deposition techniques other than sputtering" for depositing TiN. The specific citation by Fortin (4:49-56) is:

> The invention is not limited to any particular sputtering process, and further is applicable to TiN deposited by physical vapor deposition techniques other than sputtering. For example, pulsed laser deposition and other evaporation techniques can be used. See 'Handbook of Semiconductor Manufacturing Technology' (2000), cited above, pages 395-413, incorporated herein by reference.

But referring the reader of the patent to a reference for information on specific examples is not the same as relying on it for the underlying definitions of specific terms, here PVD and CVD. Had Fortin intended to rely on the Nishi Handbook for definitions, then presumably he would have cited specifically to descriptive statements, and in a way to make such an intent clear, such as when introducing the terms or explaining their relationship to his invention. For example, Fortin stated at the outset that, "The present invention relates to the physical vapor

deposition of titanium nitride" (1:8-9), which would have been a logical place for him to cite specific passages of Nishi, which he did not do, had he intended to rely on it to define PVD. To the contrary, leaving no doubt about what he meant, Fortin gave his own descriptions of the terms PVD and CVD in the prosecution (Ex. H to DI 86 at 9 and quoted above), which are different from the descriptions in the cited chapter of the Nishi Handbook. Fortin's descriptions were the descriptions that the Patent Office relied upon in deciding to issue the Fortin patent. [1]

Arguing that the Court should not adopt Freescale's definitions (based on Fortin's words) of PVD and CVD, ProMOS asserts that Freescale ignores the "essential concept" of flux by omitting from PVD the purported notion of "an overall net 'flux' of individual species" (DI 84 at 35) and from CVD, that there is no "preferred direction of flux" (DI 84 at 37). Not only will ProMOS's construction baffle the jury (what is "flux"? what is flux's "direction"?), it is not supported. "Overall net flux" as required for PVD is ProMOS's made-up interpretation and ProMOS does not cite any place in the chapter (or elsewhere) where that interpretation is supported. Similarly, ProMOS, not the chapter's author (S. M. Rossnagel), says that "preferred direction of flux" distinguishes PVD from CVD and ProMOS again does not cite support. Notably, Rossnagel makes clear in a subsequent publication that ProMOS's interpretation of Rossnagel's description of PVD as requiring directional flux (and as a distinguishing feature

[1] The only differences between Freescale's definitions of PVD and CVD and Fortin's descriptions in the prosecution are: (a) Fortin said that release of material in PVD is "largely" by physical mechanisms; and (b) Freescale has made explicit the points that material is built up in a deposition process and that a vapor is involved in PVD. It is not clear why Fortin hedged with the word "largely," as PVD clearly requires that the mechanism for releasing material be physical. The examples of PVD cited by Fortin in the patent (sputtering, pulsed laser, and other evaporative techniques) involve only a physical mechanism as the chapter of Nishi cited by Fortin makes clear (4:49-56). The requirement that a deposition process build up or accumulate material would make clear to a jury the basic point of a deposition process. That a vapor is involved in PVD is also basic, as previously discussed.

between PVD and CVD) is wrong. Although he describes evaporation as one PVD method of directionally controlling the flux, Rossnagel emphasizes that sputter deposition, which he characterizes as a PVD method, is nondirectional (Ex. K at S86):[2]

> Sputter deposition, by comparison, is almost always in a very *nondirectional* deposition configuration. . . . The result is that sputter deposition of atoms results in arrival directions for the depositing atoms which range from near-normal incidence to grazing . . . .[3]

ProMOS apparently does not dispute that, in PVD and CVD as with other deposition processes, material must be built up, as Freescale's definition explicitly states. Yet ProMOS's definitions would deliberately obscure that point, apparently so that ProMOS may later argue otherwise. Further, ProMOS's definition of PVD omits the fundamental requirement that the mechanism of release from the starting material must be physical, instead focusing on a general notion of how material, after having been released, is deposited ("atomically by means of fluxes of individual neutral or ionic species"). That notion, however, applies as well to CVD and so does not distinguish the term PVD from CVD (as Fortin had to do to obtain his patent over the

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[2] ProMOS argues (DI 84 at 36) that the definition of PVD as Freescale originally proposed it, which had an additional sentence, would have read out the preferred embodiment of so-called "reactive sputtering." That issue is irrelevant (as well as moot) as Freescale has not argued for a construction that would rule out reactive sputtering. Reactive sputtering is a form of sputtering in which a solid titanium target is bombarded to physically dislodge surface atoms of titanium into a vapor phase including nitrogen ambient for subsequent accumulation on the deposition surface. As noted in Freescale's opening brief, sputtering is unquestionably a form of PVD and Freescale's definition includes sputtering (DI 85 at 14-15).

[3] Rossnagel also gave a more comprehensive explanation of PVD which comports with Fortin's, its customary meaning and Freescale's definition (Ex K at S74):

> Typically these atoms are removed from a solid or liquid source, transit an evacuated chamber, and impinge on a solid surface at which point the atoms stick and form a film. The means to remove the atoms from the original source can be by thermal heating of the source [evaporation] or energetic particle bombardment by electrons, atoms, ions, molecules, or photons.

prior art).[4] Only Freescale's definition accounts for the essential aspects of the respective processes: in the customary understanding of the term PVD, material is physically released into vapor form before being deposited and, in CVD, a vapor undergoes a chemical reaction that enables the material being deposited to be released from its starting chemical species and accumulate on the surface. All these concepts are critical and should be reflected in the definitions of PVD and CVD that the Court adopts.

B. The Inter-Relationships of PVD, CVD and Sputtering

ProMOS argues that it is "circular" and "backwards" (DI 84 at 35, 37) to include in the definitions of PVD and CVD the inter-relationship of the terms, i.e. that the two terms are mutually exclusive. But the point of the claim construction exercise is to construe the claim terms as the inventor meant them so that, when the jury (or the Court) applies the claims for purposes of infringement and invalidity, the inventor's intent is made clear. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005); *see also Renishaw PLC v. Marposs Societa' Per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998) ("[T]he interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim.").

Here, clarifying the relationship of PVD and CVD was important to the inventor to obtain his patent. To distinguish his invention from the patent to Fiordalice, Fortin argued that Fiordalice deposits TiN by CVD whereas Fortin deposits TiN by PVD. After noting the important differentiating characteristics of the two processes (incorporated in Freescale's definitions), Fortin made a final clarifying point to be absolutely sure that there could be no

[4] The statement that material is deposited "atomically by means of fluxes of individual neutral or ionic species" does not differentiate PVD from CVD. Depositing "atomically" simply means one atom at a time; neutral and ionic species are the only possibilities.

doubt about the distinction: "In any event, CVD is not PVD or a type of PVD" (DI 86, Ex. H at 9) (original emphasis). Given Fortin's belief that this degree of clarity was necessary for the examiner to fully understand the terms and how his invention differed from the prior art, then that degree of clarity is just as important now to help the jury. There can be no legitimate reason not to include that unequivocal clarification in the claim constructions.

Contrary to ProMOS's assertion (DI 84 at 35-36), there is nothing improper about including in a definition what the term is not. This Court has done so. *Bayer Healthcare LLC v. Abbott Labs.*, 2005 WL 2346890 at *9 (D. Del. Sept. 26, 2005) ("gear" construed as a "toothed machine part, such a wheel or cylinder, that meshes with another toothed part, to transmit motion or to change speed or direction, *and which excludes a chain.*"); *Applied Sci. & Tech., Inc. v. Advanced Energy Indus., Inc.*, 204 F. Supp. 2d 712, 715 (D. Del. 2002).[5] In *Bayer*, "Bayer clearly and unmistakably distinguished chains from gears." *Bayer* at *9. Fortin too "clearly and unmistakably distinguished [PVD] from [CVD]" and the construction of the terms should therefore reflect that unmistakable distinction.

C. Sputtering

ProMOS asserts that Freescale's definition is incorrect in placing sputtering as one type of PVD (DI 84 at 39). Asserting that "the sputtering process is characterized by the removal of material" (*id.*), ProMOS is clearly trying to preserve the notion that "sputtering" as used by Fortin could include a process that is an etch (e.g. one not intended to build up material, but instead to remove material). This is contrary to the explicit claim language and makes no sense.

Sputtering is used in claims 2, 32, 48, and 54, where it depends from limitations requiring

[5] ProMOS's reliance on *Winn, Inc. v. King Par Corp.*, 2005 WL 2033531 (E.D. Mich. Aug. 16, 2005) is misplaced. Although that court did not include a negative in a definition (i.e., what the term did not include), the inventor had not relied in the prosecution on a negative to distinguish the term from things that were not the invention. Here Fortin did.

PVD. Thus, there can be no question that sputtering as used in those dependent claims is a type of PVD. In independent claim 25, sputtering is used to form the TiN layer and PVD is not explicitly referenced. However, not only should sputtering be read the same way in all the claims, *Phillips*, 415 F.3d at 1314, but the entire point of sputtering in claim 25 is to *form* a layer, not to *remove* one that is already there (6:35-37: "forming a titanium nitride layer over the titanium layer . . . the titanium nitride layer being formed by sputtering").

Although it is correct that sputtering connotes particular aspects of the front end of the process (i.e., the particular way material to be deposited is physically removed from the starting material – by bombarding the starting material as opposed to, for example, evaporation which is also a physical mechanism), and to that extent characterizes sputtering, unquestionably Fortin was using the term as a type of PVD.[6] Not only is that usage clear in the claims, but he emphasized in the specification that sputtering is a form of PVD: "The invention is not limited to any particular sputtering process, and further is applicable to TiN deposited by *physical vapor deposition techniques other than sputtering*" (DI 86, Ex. A at 4:49-52) (emphasis added). And during prosecution, he stated, "[e]xamples of PVD include sputtering . . ." and "sputter deposition is a type of PVD" (DI 86, Ex. H at 9, 10; *see also id.* at 11).

Ignoring Fortin's clear statements, ProMOS argues that its construction, which omits that sputtering is a deposition process (and indeed a type of PVD), is correct because its "definition is taken directly from" the Rossnagel chapter of Nishi (DI 84 at 38). ProMOS is wrong. As noted above (pp. 4-5), Fortin did not rely on the Rossnagel chapter as providing a definitional

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[6] "Sputtering" is a term that requires some context, as it is sometimes used in the context of an etch process (a "sputter etch") to clean a surface by removing material (*see* Ex. L at 108) (Exhibit L is a portion of a reference authored by Wolf, a page of which was cited in the patent, 3:54-55). But in this case, Fortin was clearly using the term as a deposition process, as made clear by the cites above and below.

description. Moreover, ProMOS's definition is only part of what Rossnagel says. ProMOS omits Rossnagel's statement that, "[t]he sputtered atoms must then move through the background gas to land at the desired sample surface," in other words, that he is referring to more than simply a removal process as ProMOS would define sputtering (DI 84, Ex. 10 at 397).

Thus, "sputtering" should be construed as "a type of physical vapor deposition in which a solid target is bombarded with high energy ions physically to dislodge the surface atoms on the target into a vapor phase for accumulation on the deposition surface without undergoing a chemical reaction."

II. ROUNDING

ProMOS's exact argument on "rounding" is unclear, but seems to be that "rounding" is understood with reference to the "rounded edge shown in Figure 5" of the patent, and is determined not by a measurement but rather by use of particular plasma etch process parameters described in the patent (DI 84 at 34). Specifically, ProMOS refers to the result of milling away (i.e. etching) as "rounding" and then ties "rounding" in Figure 5 to the specific process described for the plasma etch: "One of ordinary skill in the art readily understands that exposing the silicon dioxide dielectric layer 110 to RF plasma in an argon atmosphere for 10 seconds produces exactly the type of rounded edge that is shown in Figure 5" (*id*.).

But this assertion is mere lawyer argument, as ProMOS fails to explain or support how one of ordinary skill in the art would be led to make this connection, and how its reading would allow generalization such that a competitor who carried out different etch parameters would understand the term and know whether what it did infringes. Notably, ProMOS does not argue that "rounding" should be defined as the result of a process using an etch with the particular parameters it cites. Accordingly, the term should be held to be insolubly indefinite.

THE CHAN PATENTS

Freescale's constructions for each of the disputed Chan patent claim terms adhere to the methodology mandated by the Federal Circuit in *Phillips*, 415 F.3d at 1313-17. Freescale's proposed constructions are supported by the intrinsic record -- the claims, specifications, and prosecution histories.

ProMOS's constructions, in contrast, largely ignore the specification and completely ignore the prosecution histories, contrary to *Phillips*. *Id.* Instead, ProMOS relies on extrinsic evidence and, mostly, unsupported lawyer argument. ProMOS understandably wants to avoid the context of the Chan patents because it needs to in order to seek constructions that go far beyond anything that Chan actually invented. However, "[t]he patent system is based on the proposition that claims cover only the invented subject matter." *Id.* at 1321 (citing *Merrill v. Yeomans*, 94 U.S. 568, 573-74 (1876)).

ProMOS has three claim construction goals: (1) avoiding the "chip" limitation that is applicable to all claims; (2) preserving an ability to twist claim constructions at trial when presenting its infringement case to the jury; and (3) avoiding the indefinite terms that doom many of the Chan claims. Each fails under established law.

I. CHAN TERMS IN WHICH PROMOS'S GOAL IS TO AVOID THE "CHIP" LIMITATION

Although there are various key points in dispute, a major point of contention -- and one whose resolution will drive a number of claim constructions -- is whether Chan's invention covers products where the only cache that is used is one that is internal (as opposed to external) to a microprocessor. As demonstrated in Freescale's opening brief, and below, Chan described and claimed a particular system which used an external cache and an external cache controller to accelerate the microprocessor's overall performance. *See* DI 85 at 25-32.

Indeed, the problem Chan was trying to solve is exacerbated by the use of internal caches. Chan's precise solution therefore was to have the microprocessor use a particular external cache, the Chan cache chip, and to use the external Chan cache in a certain way, so that the microprocessor did not have to wait to provide or obtain information from the system memory before it could continue performing its operations. Because Chan's invention has no applicability to internal cache-only situations, the claim language, all embodiments in the specification, and the file histories -- in short, all of the intrinsic evidence -- describe Chan's invention as being a system that uses only an external cache. Indeed, there is not a *single* piece of intrinsic evidence where Chan describes his invention as using a cache or cache controller that is on the same chip as (*i.e.*, internal to) the microprocessor.

A. Chan's Invention Is Not Applicable To An Internal Cache

The Chan patents address how quickly a microprocessor can access (*i.e.*, send data to ("write") or obtain data from ("read")) the slower system (or "main") memory that is external to (*i.e.*, not on the same chip as) the microprocessor. ('709 at 3:64-68.) A microprocessor functions by obtaining data from system memory, internally processing that data, and outputting that processed data back to system memory. The microprocessor is capable of inputting or outputting data much faster (*e.g.*, once per clock cycle) than system memory can provide or receive the data (*e.g.*, once every several clock cycles). ('709 at 2:8-15.) Consequently, when the microprocessor is connected (or "coupled") directly to system memory, as illustrated in Fig. A below, it cannot input or output data as quickly as it is technologically capable. (*Id.*)

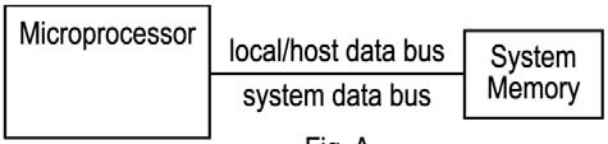

Fig. A

Instead, inputting and outputting can proceed only at the speed that system memory can provide

or receive the data, which is only once every several clock cycles, causing the microprocessor to wait for the data input or output operation to complete before performing other operations. (*Id.*)

Chan's solution to this problem is to disconnect (or "decouple") the microprocessor from the system memory (*i.e.*, the direct connection between the microprocessor and system memory is broken). ('709 at 3:64-68.) As shown in Fig. B, the microprocessor is coupled directly to an external Chan cache chip which, in turn, is coupled to the system memory. ('709, Fig. 6-7, 32.)

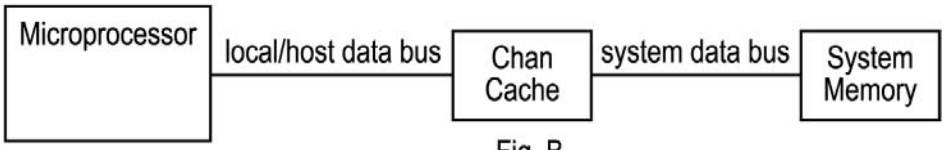

Fig. B

The Chan invention allows the microprocessor to input or output data to the much faster external Chan cache at a faster rate (*e.g.*, once every clock cycle) instead of the slower rate (*e.g.*, once every several clock cycles) that would be required if the microprocessor were coupled directly to the system memory. ('709 at 73:7-16.) At the same time, data can be communicated between the external cache and the system memory along a different line ("system data bus") without affecting the speed at which the microprocessor can perform its operations. ('709 at 3:64-4:3.)

As illustrated in Fig. C, if the Chan cache were internal to the microprocessor, as ProMOS's litigation-driven position now urges, the Chan solution of decoupling the microprocessor from the system memory could not be implemented, and Chan's objective of preventing the system memory from slowing down the microprocessor could not be achieved.

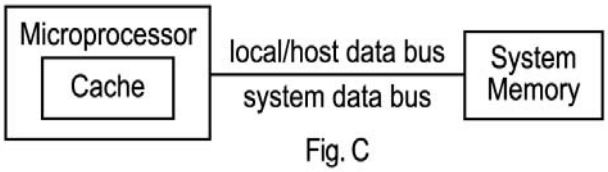

Fig. C

Instead, when the microprocessor, for example, had to send data to or get data from the system memory because that data had been processed or did not already exist in the internal cache, the

microprocessor would be forced to slow down to operate only at the speed at which system memory could receive or provide the data, which is once every several clock cycles, rather than the much faster rate achievable when the Chan external cache is used to decouple the microprocessor from the system memory. Because the problem addressed by the Chan invention, and the Chan solution to that problem, are both probative of the scope of the Chan claims, the Chan claims should be limited to cache memory chips and cache controller chips that are external to the microprocessor.[7]

B. The Chan Claims Are Directed To Cache Memory External To A Processor

The Chan claim language is directed to, and makes sense only in the context of, external cache memories. For example, claim 1 of the '709 patent (all the claims are similar in this regard) claims a "cache memory apparatus" with, *inter alia*, a host port (for communications between the cache and the microprocessor), a system port (for communications between the cache and the system memory) and a random access memory (for storing the data in the cache). As conceded by ProMOS at page 5 of its opening brief, the cache "acts as an intermediary between the host CPU [processor] and the system memory." (DI 84 at 5.) This "intermediary" must be external to the microprocessor because the cache contains a host port (akin to a doorway, as discussed below) for permitting data to exit the cache and get transmitted to the microprocessor and for permitting data from the microprocessor to enter the cache. There would be no need for a host port if the cache were internal to the microprocessor.

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[7] *See CVI/Beta Ventures, Inc. v. Tura LP*, 112 F.3d 1146, 1160 (Fed. Cir. 1997) ("In construing claims, the problem the inventor was attempting to solve, as discerned from the specification and the prosecution history, is a relevant consideration"); *Union Oil Co. v. Atlantic Richfield Co.*, 208 F.3d 989, 996 (Fed. Cir. 2000) (affirming construction limiting claims to cover only ordinary automotive fuels, as opposed to fuels that could conceivably be used in automobiles, based on the specification's description of the problem addressed by the invention).

C. The Specification Describes "The Invention" As An External Cache Chip

As discussed in Freescale's Opening Brief at pp. 25-32 and 36-37, Chan consistently referred to his invention as a cache memory "chip" external to the microprocessor chip.[8] Because Chan consistently described his patented cache memory as a memory chip, the claim terms "cache memory" and "cache memory apparatus" cannot encompass internal caches, which are not memory "chips." Claim terms should be construed commensurate with, and not broader than, the invention described in the intrinsic evidence. *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Group, Inc.*, 262 F.3d 1258, 1271 (Fed. Cir. 2001) ("[W]hen a patentee uses a claim term throughout the entire patent specification, in a manner consistent with only a single meaning, he has defined the term by implication." (internal quotations omitted)).[9]

According to the Supreme Court, and as recently reiterated by the Federal Circuit – "[t]he patent system is based on the proposition that claims cover only the invented subject matter." *Phillips*, 415 F.3d at 1321 (citing *Merrill v. Yeomans*, 94 U.S. 568, 573-74 (1876)). The Chan specification consistently and exclusively described his invention as using a cache memory chip and a cache controller chip external to the microprocessor. Chan was clear as to what he understood his invention to be. *See id.* at 1317. ProMOS cannot now improperly stretch the invention Chan described and claimed to include something that Chan nowhere invented or described in order to manufacture an infringement position.

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[8] Chan used the term "chip" to describe his invention over thirty times in the specification.

[9] *See, e.g.*, *Nystrom v. Trex Co.*, 424 F.3d 1136, 1142-45 (Fed. Cir. 2005) (limiting the claim term "board" to "wood decking materials cut from a log"); *AquaTex Indus., Inc. v. Techniche Solutions*, 419 F.3d 1374, 1380-82 (Fed. Cir. 2005) (limiting "fiberfill batting material" to synthetic materials, and excluding natural fibers, based on the language of the claims, written description, and prosecution history); *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1258, 1370-71 (Fed. Cir. 2003) (Limiting the invention to flooring panels with "play" because "the '907 specification read as a whole leads to the inescapable conclusion that the claimed invention must include play in every embodiment.").

D. The Chan Prosecution History Limited The Invention To External Chips

It is clear from the prosecution history that neither the cache memory nor the cache controller can be internal to the microprocessor. To persuade the Patent Office to issue his '241 patent over the prior art, Chan represented to the Patent Office that the cache controller, cache memory, microprocessor and system memory of his invention were separate and independent:

> The present invention relates to a computer system which includes a cache memory system and a cache controller which decouple a main memory subsystem from a host data bus. More specifically, the present invention, as set forth in independent claim 4 [issued claim 1], relates to a computer system which includes a host microprocessor, a system memory, a dual port cache memory and a cache controller. . . . The cache controller and the cache memory are connected in parallel between the host microprocessor and the system memory, thus allowing the host microprocessor to be decoupled from the system memory.

(Ex. 22, '241 File History, Paper 12 at 9 (emphasis added).) In fact, it would be impossible for the structure that Chan described to be internal to the microprocessor--an internal cache controller or cache memory could not be connected in parallel between the microprocessor and system memory. Not only did Chan tell the patent office that the controller and cache memory had to be external, he also distinguished his invention from the prior art on that basis:

> Holland et al. does not disclose or suggest . . . connecting a cache controller and a cache memory in parallel between a host microprocessor and a system memory, thus allowing the host microprocessor to be decoupled from the system memory.

(*Id*. at 11.) Having persuaded the Patent Office to issue his patent on this basis, Chan is estopped from "taking back" his representations now and arguing that the cache memory and cache controller can be internal to the microprocessor.[10]

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[10] *Seachange Int'l, Inc. v. C-Cor Inc.*, 413 F.3d 1361, 1372-73 (Fed. Cir. 2005) ("Where an applicant argues that a claim possesses a feature that the prior art does not possess in order to overcome a prior art rejection, the argument may serve to narrow the scope of otherwise broad claim language."); *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing the claim is to 'exclude any interpretation that was disclaimed during prosecution.'").

E. The Advantages Of The Chan Patents Cannot Be Met By An Internal Cache

The Chan cache memory was designed to allow the microprocessor to operate over the host bus at its bus speed without having to wait for delays caused by the speed limitations of the system memory, and to allow the system memory to operate at its lower bus speed on the system data bus. (*See* '709 at 4:2-3; 73:7-12.) In that regard, the Chan specification provides a detailed discussion of several "advantages" of the Chan external cache memory system, which cannot be achieved with an internal cache:

> (1) simplifying computer system design by interfacing with Intel microprocessors in the same way that conventional SRAM chips interface with Intel microprocessors ('709 at 73:3-6);
>
> (2) decoupling external system memory from the microprocessor by decoupling buses external to the microprocessor ('709 at 73:7-12);
>
> (3) hiding system memory accesses from the microprocessor ('709 at 73:12-16);
>
> (4) allowing multiple Chan cache memory chips to be used in parallel to increase the number of bytes of data that can be sent to the microprocessor at a given time ('709 at 73:17-26);
>
> (5) providing particular architectural features that speed up microprocessor operations ('709 at 73:27-42);
>
> (6) allowing for microprocessor upgrade without changing the system memory design ('709 at 73:43-58);
>
> (7) providing particular architectural features that prevent slower system memory from slowing down the microprocessor ('709 at 73:66–74:3);
>
> (8) providing an architecture that allows for full use of the Intel 386 microprocessor features ('709 at 74:3-19); and
>
> (9) providing an architecture that allows for full use of the Intel 486 microprocessor features ('709 at 74:20-31).

Where, as here, the advantages of the invention are unachievable without a particular limitation, the claims should be construed to include that limitation.[11]

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[11] *Nystrom*, 424 F.3d at 1143-45 (limiting "board" to only those boards cut from logs because stated advantage of reducing the amount of scrap in the outermost boards cut from a log was unachievable unless the board was cut from a log).

F. A Person Of Ordinary Skill In The Art Would Recognize That Chan's Cache Chip, Controller Chip, Processor Bus, System Bus And System Memory Were All External To The Microprocessor

The Chan patents disclose a cache controller chip and a cache memory chip designed for use in a particular computer system configuration with two specific microprocessors, the Intel 80486 and 80386, the only two microprocessors mentioned in the patent. As shown in Figure 1-1 below, the Intel computer system configuration contains a microprocessor, two buses that are external to the microprocessor (i.e., both a processor bus and a system bus) and system memory. (Ex. 3, at 1-9).[12] This is the precise configuration described in the Chan patents.

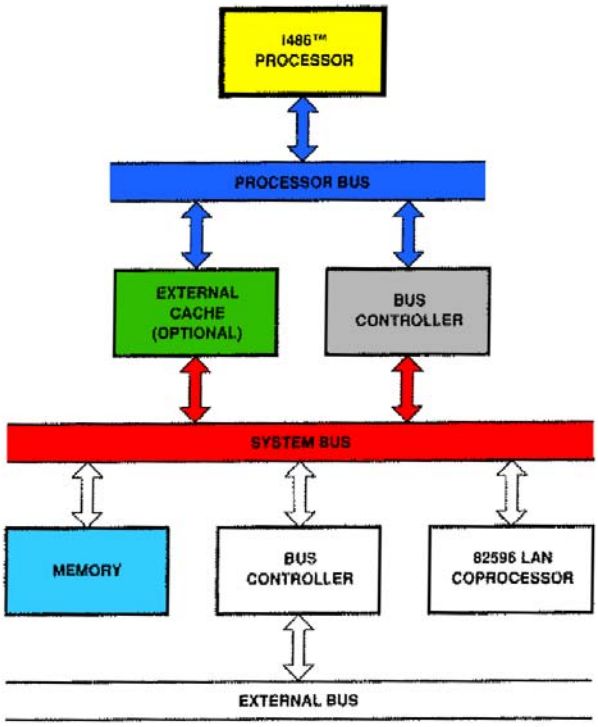

Figure 1-1. A Typical i486™ Processor System

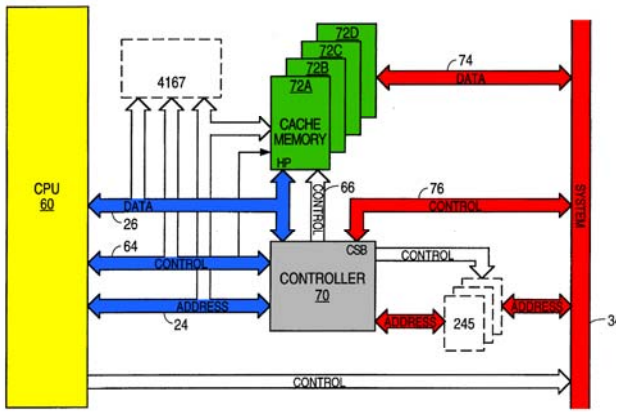

FIG. 7

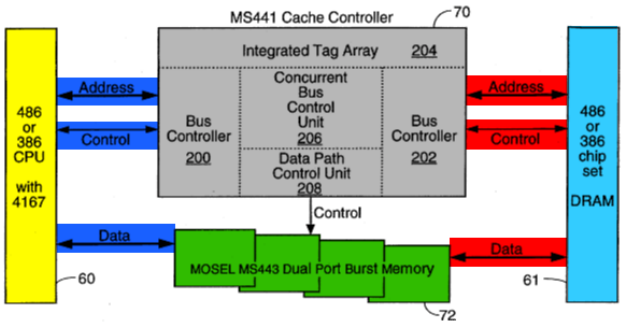

FIG. 32

As illustrated in the side-by-side comparison of Intel Figure 1-1 and Chan patent Figures 7 and 32, there is one-to-one correspondence between the devices in the Chan computer system

[12] Chan submitted the *Intel i486 Microprocessor Hardware Manual* to the Patent Office as prior art to the Chan patents.

figures and the devices in the "Typical i486 Processor System" depicted in Intel Figure 1-1.[13] The CPU 60 of Figs. 7 and 32 correspond to the i486 Processor of Intel Figure 1-1. Similarly, the data 26, address 24, and control 64 buses of Figs. 7 and 32 correspond to the Processor Bus of the Intel figure. Likewise, the data 74, address, control 76, and system 34 buses of Figs. 7 and 32 correspond to the Intel System bus. Also, the MOSEL MS443 Dual Port Burst Memory Chip 72 of Fig. 32 and the cache memory chips 72A, 72B, 72C, and 72D of Fig. 7 correspond to the External Cache of the Intel figure. In addition, the MS 441 cache controller chip 70 of Fig. 32 and the controller chip 70 of Fig. 7 performs the functions of the upper Bus Controller of the Intel figure. Finally, chip set DRAM 61 of Fig. 32 corresponds to Memory in the Intel figure.

The Intel reference manual reaffirms that the Processor Bus, System Bus, External Cache, Bus Controller and Memory are all separate from and external to the microprocessor. Figure 1-1, for example, specifically recites that the cache is an optional external component. The Intel reference manual, also, specifically instructs that the Processor Bus is connected to the pins on the microprocessor chip and therefore must be external to the microprocessor chip:

> The processor bus is the set of pinout signals on the i486 processor chip. It is the bus through which the processor communicates with other devices in the system. The signals on the bus are classed by their functions, which include . . . control, address and data

(Ex. 3 at 3-1.) Because the other components interface with the Processor Bus and/or the External Cache, and not directly with the i486 microprocessor, they also must be external. A person of ordinary skill in the art, with knowledge of the prior art "Typical i486 Processor System" would easily recognize that the Chan patents are directed to that configuration, and would therefore conclude that the Chan patents are directed to a cache memory chip and a cache

[13] The three Chan figures depicting the '241 patent computer system are Figs. 6, 7 and 32. Fig. 6 shows the system with a 386 microprocessor as the CPU, while Fig. 7 shows a 486.

controller chip that are separate from and external to the microprocessor chip.[14]

G. Chan Did Not Enable Internal Caches

In support of its erroneous contention that the Chan invention is also applicable to internal caches, ProMOS relies on a statement in the Background of the Invention section that recognizes the non-remarkable fact that internal and external caches existed in the prior art. The Federal Circuit previously provided guidance for situations such as this.

In *Wang Laboratories, Inc. v. America Online, Inc.*, 197 F.3d 1377 (Fed. Cir. 1999), the Federal Circuit held that even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass a feature in question, that feature is outside the reach of the claims when there is no written description or enablement of the feature -- even when the feature is mentioned in the Background of the Invention. In *Wang*, the parties agreed that in general usage the claim term "frame" could be applied both to "bit-mapped display systems" and to "character-based systems." *Id*. at 1381. The court, however, construed the claims as limited to character-based systems because the "only system that [was] described and enabled" in the patent specification "use[d] a character-based protocol." *Id*. at 1382. The court held that references to bit-mapped protocols in the "Background of the Invention" section were merely acknowledgments of the state of the art, and not an enlargement of the invention described in the patent, and did "not describe them as included in the applicant's invention." *Id*.

Likewise, in this case, Chan's statement in the Background of the Invention section that internal caches existed in the prior art was merely an acknowledgment of the state of the art and does not describe internal caches as being part of the Chan invention. The Chan cache memory

[14] *See Phillips*, 415 F.3d at 1321 ("We have made clear, moreover, that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.").

chip and cache controller chip are the only items that are described and enabled in the patent specification. There is no discussion in the specification or anywhere else in the intrinsic evidence of how to implement an internal cache or any drawings depicting an internal cache.[15]

H. CHAN CLAIM CONSTRUCTIONS

ProMOS impermissibly ignores the Federal Circuit's mandate in *Phillips* and other precedent by: (1) construing terms out of context solely using dictionaries and other extrinsic sources and ignoring the specification and the prosecution history; (2) attempting to require the jury to construe other claim terms by arguing construction is not necessary; and (3) for the means-plus-function terms, manufacturing structure not clearly linked in the specification to allegedly perform the specified function. ProMOS's improper approach should be rejected.

1. "cache memory apparatus" / "cache memory" - '709 claims 1, 13, 17, 22 and '241 claims 1, 15, 16

Freescale	ProMOS
a memory chip that is external to the CPU chip	"cache memory apparatus" does not need construction. "cache memory" = a small block of high speed memory associated with a computer processor/microprocessor (CPU)

Freescale agrees with ProMOS that a cache memory can be a small block of high speed memory, and that once "cache memory" has been construed, the meaning of "cache memory apparatus" will be clear. (*See* ProMOS's Opening Br., DI 84 at 25). ProMOS's proposal does not go far enough, however, because it (intentionally) avoids what Chan actually invented and disclosed, which is a cache memory chip. The principal dispute here is whether the "cache memory apparatus" and "cache memory" must be external to the CPU chip (Freescale's

[15] In addition to running afoul of the "enablement" requirement in § 112 ¶ 1, allowing the '709 and '241 patents to cover an internal cache would violate the "written description" requirement. *See Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563 (Fed. Cir. 1991); *Reiffin v. Microsoft Corp.*, 214 F.3d 1342, 1345 (Fed. Cir. 2000) ("The purpose of this provision is to ensure that the scope of the right to exclude, as set forth in the claims, does not overreach the scope of the inventor's contribution to the field of art as described in the patent specification."); *Gentry Gallery, Inc. v. Berkline Corp.*, 134 F.3d 1473 (Fed. Cir. 1998).

proposal) or can also be construed to cover caches that are internal to the processor (ProMOS's proposal).[16] As demonstrated in Freescale's opening brief and above, Freescale's construction is correct because the only device that Chan described and enabled in his patents is an external cache, the object of the Chan patents can only be accomplished by an external cache, and the alleged advantages of the Chan patents can only be achieved with an external cache.[17]

ProMOS's construction, once again, seeks to cover subject matter Chan clearly did not invent and, therefore and not surprisingly, lacks support in the intrinsic evidence. As discussed above in Part I.G, ProMOS's only alleged record support comes from the "Background of the Invention" section and, even this background discussion does not support ProMOS's construction.[18] Moreover, the extrinsic evidence on which ProMOS relies, a 2004 publication, actually supports Freescale's, and not ProMOS's, construction.[19] That publication instructs, on a page that ProMOS failed to cite, that the performance of a CPU with an internal cache can be improved by adding an external cache device – "[e]ven greater performance can be achieved by building an off-chip cache of faster memory outside the processor . . . to accelerate the access time of SDRAM during on-chip misses"[20] – in other words, exactly what Chan did. As discussed above in Part I.E. accelerating the access time of the SDRAM system memory during on-chip misses (i.e., when the internal cache, if there is one, does not contain the data sought by the microprocessor) is the problem identified and solved by Chan's invention. And, as Chan

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16 Freescale also believes the "associated with" language is vague and will confuse the jury.

17 *See supra* Part I.A-G and Freescale's Opening Br., D.I. 85 at Part III; IV.A.

18 *See* ProMOS's Opening Br. at 6, 11 (citing 2:60-65 and 2:66-3:1.)

19 Many of the extrinsic sources on which ProMOS relies are from the wrong time frame, which, in the case of Chan, is June 1990. *See, e.g., PC Connector Solutions LLC v. SmartDisk Corp.*, 406 F.3d 1359, 1363 (Fed. Cir. 2005) (noting that the meaning of claim "must be interpreted as of [the] effective filing date" of the patent application).

20 *See* Ex. 6 to ProMOS's Opening Br., P. Genua, *A Cache Primer* (Oct. 2004) at 6.

recognized and confirmed by the 2004 publication, using an external (not internal) cache to accelerate the operations and decouple the microprocessor from the system memory is the solution to Chan's problem.[21]

2. "cache controller" / "controller" - '241 claims 1, 15 and 16

Freescale	ProMOS
a chip that controls a cache memory chip	circuitry that controls the transfer of data or other information to and from cache memory

ProMOS's construction for these terms is overbroad and, significantly, again ignores that what Chan described and enabled as his invention was a cache controller chip that was separate from the microprocessor chip. First, ProMOS's construction is so broad that it can actually cover a microprocessor.[22] This is a nonsensical result because the claimed "controller" is designed to work with – and not be – a microprocessor; indeed, the point of a cache controller is to control the transfer of information between a cache and a microprocessor. ('709 at 6:55-60.)

Moreover, ProMOS's construction ignores the fact that every embodiment, every description, and every figure of the cache controller in the Chan specification is of a cache controller chip that is separate and external from the microprocessor chip and the cache memory chip. (*See e.g.*, Figs. 13, 14, 32 and 33 and DI 85 at 33-34.) Patent Figures 14 and 32, for example, identify the specific cache controller chip as the MS441 (shorthand for the MOSEL MS82C441). The Chan specification specifically acknowledges that the claimed cache

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[21] Under Federal Circuit caselaw, ProMOS cannot construe these terms beyond Chan's actual invention to allow it to argue infringement where none exists. *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001); *Netword, LLC v. Centraal Corp.*, 242 F.3d 1347, 1352 (Fed. Cir. 2001) ("Although the specification need not present every embodiment or permutation of the invention and the claims are not limited to the preferred embodiment of the invention, neither do the claims enlarge what is patented beyond what the inventor has described as the invention.").

[22] Moreover, ProMOS did not provide support for its use of "circuitry" in its construction. The intrinsic evidence on which ProMOS relies merely supports the unremarkable proposition that the controller performs a "control function", a proposition with which Freescale agrees.

controller is an external chip by identifying its terminal pins; the cache controller obviously would not need pins to communicate with the microprocessor if it were internal to the microprocessor.[23] Because Chan throughout the specification described the cache controller as being a chip separate from the processor and the cache memory chip, Chan has defined his cache controller as being an external chip.[24] Freescale's proposed construction should be adopted.

3. "system memory" - '241 claims 1, 15 and 16

Freescale	ProMOS
main memory of a computer system that is external to the CPU chip	Main memory of a computer, relatively larger and slower than cache memory

Once again, the principal debate here is whether the main memory, like the cache memory and cache controller, are external to the host processor (Freescale's proposal) or can be internal to the host processor (ProMOS's proposal). Again, however, every embodiment, every description, and the only figure showing system memory in the Chan specification is of system memory that is external to the microprocessor chip and the cache memory chip – there simply is

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[23] *See, e.g.*, '709 at 5:47-48 ("FIG. 33 is a diagram showing functional block pin groups of cache controller 70."); '709 at 10:47-52 ("The burst RAM cache memory 72 and controller 70, in accordance with the invention, control the paths of data in response to various control signals. These signals, along with the terminal pins of cache memory 72 and controller 70 from which they are provided, are listed below in Tables I and II."); '709 at 50:46-49 ("The controller 70 presents a very 486 CPU-like interface to system logic. The great majority of system interface pins have the same name and functionality as their 486 CPU counterparts."); '709 at 50:61-63 ("On the system side, the controller 70 has an identical list of pins as does the i486 CPU, except for the following pins . . ."") (emphases all added).

[24] *See, e.g., Bell Atl.*, 262 F.3d at 1271 ("when a patentee uses a claim term throughout the entire patent specification, in a manner consistent with only a single meaning, he has defined the term by implication" (internal quotations omitted)); *see also Innovad Inc. v. Microsoft Corp*, 260 F.3d 1326, 1332 (Fed. Cir. 2001) (construing the term "dialer" as having no keypad, where "[r]epeatedly, the specification emphasizes that 'the dialer has no keypad.'"); *Laitram Corp. v. Morehowe Indus., Inc.*, 143 F.3d 1456, 1463 (Fed. Cir. 1998) (finding "driving surface" limited to flat driving surfaces because "nothing in the written description suggested that the driving surfaces can be anything but flat" and "the benefits of having flat driving surfaces are stated in the 'Summary of the Invention' portion of the written description").

no support to the contrary anywhere in the intrinsic evidence. (*See, e.g.*, Fig. 32l DI 85 at 25-32.) As discussed above in Part I.F, a person of ordinary skill in the art would view system memory as being separate from the microprocessor chip. Freescale's construction for this term should be adopted.

4. "host processor" / "host" / "host microprocessor" - '241 claims 1, 10, 15, 16

Freescale	ProMOS
a single chip central processing unit (CPU)	CPU associated with one or more cache memories

ProMOS has mischaracterized Freescale's position. As discussed in Freescale's Opening Brief, Chan uses these terms interchangeably in the specification to describe a microprocessor. (DI 85 at 45.) Thus, Freescale's construction is that these terms should be equated with a microprocessor, which is a single-chip central processing unit ("CPU").

ProMOS has proposed a construction that, once again, has no support in the specification or anywhere else in the intrinsic evidence to impermissibly stretch the claimed cache memory and cache memory apparatus into being internal to the microprocessor. For the reasons discussed above, ProMOS's position should be rejected.

II. TERMS IN WHICH PROMOS'S GOAL IS TO PRESERVE AN ABILITY TO TWIST ITS CLAIM CONSTRUCTIONS AT TRIAL

When offering constructions, ProMOS at times avoids the specification completely and instead simply (and improperly) construes claims terms in the abstract. For example, as demonstrated in Freescale's Opening Brief, the Chan specification uses the term "buffering" in a specific way to give that term a special meaning. (DI 85 at 45.) ProMOS conveniently and impermissibly simply ignores this intrinsic evidence, and instead applies a dictionary definition to this term. This approach to claim construction was expressly rejected by the Federal Circuit, and should be rejected in this case also. "The main problem with elevating the dictionary to such prominence is that it focuses the inquiry on the abstract meaning of words rather than on the

meaning of claim terms within the context of the patent. Properly viewed, the "ordinary meaning" of a claim term is its meaning to the ordinary artisan after reading the entire patent. *Phillips*, 415 F.3d at 1321.

To dodge fatal indefiniteness issues and preserve an ability to twist claim constructions at trial, ProMOS at other times simply argues that certain other key claim terms need not be construed at all. For example, ProMOS candidly admits that the claim term "operably decoupled" does not have a readily understood meaning (DI 84 at 22), yet ProMOS argues that the Court nevertheless should not construe it and does not even bother to try to offer a construction for this meaningless term.

Controlling precedent, however, dictates that the Court should construe contested claim terms because otherwise the jury will concededly be left to guess what the term means, without regard to the canons of claim construction, and meaningful appellate review will be frustrated. "[T]he trial court in a patent case must at minimum take steps to assure that the jury understands that it is not free to consider its own meanings for disputed claim terms . . . ." *Sulzer Textil A.G. v. Picanol N.V.*, 358 F.3d 1356, 1366 (Fed. Cir. 2004); *see also Graco, Inc. v. Binks Mfg.*, 60 F.3d 785, 791 (Fed. Cir. 1995).

In *Toro Co. v. Deere & Co.*, the Federal Circuit remanded claim construction where the trial court had stated that the claim terms received their "ordinary meaning", but failed to articulate that meaning. 355 F.3d 1313, 1319 (Fed. Cir. 2004). Moreover, that term must be construed not as a layperson may generally understand that term in a different context, but instead as it would be understood by a person of ordinary skill in the art at the time the alleged invention was made, and in the context of the entire patent. *Phillips*, 415 F.3d at 1313. Such meaning is a legal matter which this "court has the power and obligation to" decide. *Markman v.*

Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995).

A. Port Terms – Doorway To The Chips

Because it is the only way it can strain these terms into an infringement argument, ProMOS' constructions of these "port" terms impermissibly avoid the full context of specification. Instead, ProMOS takes isolated snippets from the specification out of context to support erroneous constructions for the "port" terms.

Instead of looking first at the Chan specification and other intrinsic evidence, as mandated by the Federal Circuit, ProMOS instead scoured through dictionaries to find a definition for port that it liked. Compounding this error, ProMOS then erroneously equated "port" with "interface," even though those words have different meanings. As the specification makes clear, although the terms "interface" and "port" are related, they are not synonymous. For example, Chan stated that the host port was specific structure (like a doorway) on the cache memory chip for allowing the entry and exit of data to and from the cache memory chip (much like an attached garage allows a car to enter and exit a house). ('709 at 6:58-60; Fig. 13.) In contrast, an interface was an electrical pathway between multiple devices.

According to the intrinsic evidence, the claimed "host port" is a specific point of access (i.e., the doorway) on the cache memory chip *(see, e.g.,* '709 at Fig. 6 ("HP"); Fig. 7 ("HP"); and Fig. 12A), whereas, in contrast, an interface is a "shared electrical boundary between parts of a computer system, through which information is conveyed." (i.e., the highway along which the car travels to the port of another destination) (Ex. 29, *IEEE Standard Dictionary of Electrical and Electronic Terms* 666 (5th ed. 1993).) In other words, a port can be part of an interface, but the interface needs to include all the parts that permit communication between devices (*e.g.*, a first port attached to one device, a data bus, and a second port attached to the second device) Indeed, contrary to ProMOS's assertions, the support upon which ProMOS relies does not equate

port with interface but, instead, merely recognizes that a port can be part of an interface and helps perform the interface function ("the host port 113 interfaces…" ('709 at 73:3)), but that is a far cry from saying that port is the actual interface. In fact, perhaps the most persuasive evidence of all here is the fact that Chan uses both "port" and "interface" throughout his specification, but intentionally chose "port" and not "interface" to define his invention in his claims.

Like its other litigation-driven constructions, ProMOS's use of the term interface is designed to avoid the fact that the claimed port must be located on the specific structure into or out of which data is flowing. In this case, the specifically claimed host and system ports are the points of access on the cache memory chip that permit data to be transferred into and out of the chip, and the first and second ports are the points of access on the cache controller chip for address information to flow into and out of the controller chip. Because both the cache memory chip and the cache controller chip are chips, the point of access, i.e., the ports, are the pins on those chips that allow for information to be communicated into and out of those chips.

1. "host port" and "system port" - '709 claims 1, 13, 17, 22 and '241 claims 1, 10, 16

Freescale	ProMOS
host port	
a set of pins on the cache memory chip used for the input and output of data over the host data bus	interface between a cache memory and a host processor or host data bus
system port	
a set of pins on the cache memory chip used for the input and output of data over the system data bus	interface between a cache memory and a system memory or system data bus

ProMOS's construction of "host port" and "system port" as "interface" fails to recognize how the terms are used in the specification and prosecution history. Chan repeatedly described the host port as a set of pins.[25] For the reasons discussed above and the reasons discussed in

[25] *See, e.g.*, '709 at 36:61-63 ("…allow data from the cache RAM array section 100 to bypass the read hold register set 114 and be sent to the host port data pins."); '709 at 37:1-4 ("connect the output of the read hold register set 114 to the host port 113 data pins."); '709 at (Continued . . .)

Freescale's opening brief at 39-41, Freescale's proposed constructions should be adopted.

2. "first port" and "second port" - '241 claims 1 and 16

Freescale	ProMOS
first port	
pins on cache controller chip used for the input and output of address information over the host address bus	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: "a port connected to the host address bus"
second port	
pins on cache controller chip used for the input and output of address information over the system address bus	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: "a port connected to the system address bus"

ProMOS argues that no construction is necessary for first port and second port. ProMOS has declined to propose a construction for these claim terms presumably because these terms are not used anywhere in the Chan specification. Instead, these made-up terms were invented for purposes of the claims, and added via an amendment after the Chan patents were filed. To preserve the validity of the claims containing them, these terms must find support in the Chan specification or else they will render the claims containing them indefinite. (DI 85 at 51-55.) The only plausible constructions for these terms are the constructions proposed by Freescale, which recognize that the Chan specification described the cache controller as having pins as the point of access for data input and output.[26] For all of these reasons, Freescale's proposed

(. . . continued)
39:57-59 ("The contents of write register 120 will be driven onto the system port data pins."); '709 at 69:36-39 ("[T]he system should provide even parity on the [system port] data pins during snoop write operations."); '709 at 10:47-52 ("The burst RAM cache memory 72 and controller 70, in accordance with the invention, control the paths of data in response to various control signals. These signals, along with the terminal pins of cache memory 72 and controller 70 from which they are provided, are listed below in Tables I and II with a brief description of their purposes.") (emphases all added).

[26] *See, e.g.*, '709 at 5:47-48 ("FIG. 33 is a diagram showing functional block pin groups of cache controller 70."); '709 at 10:47-52 ("These signals, along with the terminal pins of cache memory 72 and controller 70 … are listed below in Tables I and II."); '709 at 50:46-49 ("The controller 70 presents a very 486 CPU-like interface to system logic. The great majority of system interface pins have the same name and functionality as their 486 CPU counterparts."); '709 at 50:61-63 ("On the system side, the controller 70 has an identical list
(Continued . . .)

construction for these terms should be adopted or the claims containing them held indefinite.

3. "dual port cache memory" - '241 claims 1, 15 and 16

Freescale	ProMOS
a cache memory chip having a host port and a system port	a cache memory that has that has two interfaces

ProMOS's proposed construction, again, ignores the Chan specification and attempts to construe this term in the abstract, which as discussed above is improper as a matter of law. For the reasons discussed above and the reasons discussed in Freescale's opening brief at 41, Freescale's proposed construction for this term should be adopted.

B. Bus Terms – Highway Between The Chips

For the bus terms, ProMOS avoids the specification altogether and instead construes these claim terms wholly in the abstract. Instead of addressing the "host address bus" and "host data bus" terms Freescale identified for constructions, ProMOS has chosen to construe the simple word "bus" to impermissibly avoid the context of these claim terms as they are used in the specification. As discussed above, this approach to claim construction has been rejected by the Federal Circuit and should also be rejected here.

1. "host address bus" - '241 claims 1, 15, 16

Freescale	ProMOS
A set of conductors connected to the address terminal pins of a CPU chip used to transfer memory addresses from the CPU to other components of a computer system	Bus - line or set of lines used to transfer data or other information Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a bus for providing a host address.

The Chan specification uses the term "host address bus 24" interchangeably with the term "local address bus 24" and describes that "[a]ddress information is transferred between the microprocessor 60, the cache controller 70, and cache memory 72 over local address bus 24."

(. . . continued)
of pins as does the i486 CPU, except for the following pins . . .") (emphases all added).

('709 at 6:55-58.) Figure 13, which Chan describes as "illustrat[ing] the system and host interface connection pins for an 80486 computer system incorporating a cache memory 72 and controller 70 in accordance with the invention," shows that the host address bus is the interface between the ports (or pins) of the microprocessor 60, the ports (or pins) of the MS82C443 cache chip, and the ports (or pins) of the cache controller chip 70. ('709 at 4:62-64.) Freescale's construction is consistent with the term's use in the specification and should be adopted.

2. "host data bus" - '241 claims 1, 15, 16

Freescale	ProMOS
A set of conductors connected to the data terminal pins of the CPU used to transfer data to and from the CPU and other components of a computer system	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a bus for providing host data.

Freescale's proposed construction of this term should also be adopted. The Chan specification uses the term "host data bus 24" interchangeably with the term "local data bus 24" and describes that "data is transferred between the microprocessor 60, the cache controller 70, and the host port HP of the cache memory 72 over the local data bus 26." ('709 at 6:55-60.) Figure 13, which Chan describes as "illustrat[ing] the system and host interface connection pins for an 80486 computer system incorporating a cache memory 72 and controller 70 *in accordance with the invention*", shows that the host data bus is the interface between the ports (or pins) of the microprocessor 60, the host port HP (or pins) of the MS82C443 cache memory chip, and the ports (or pins) of the cache controller chip 70. ('709 at 4:62-64.) Freescale's construction is consistent with the term's use in the Chan specification and therefore should be adopted.

C. "buffering" - '709 claims 1, 13 & 22 and '241 claim 1

Freescale	ProMOS
Using a storage element (*e.g.*, memory write register) as an intermediary device to hold data temporarily while the data is waiting to be transferred from one external device (*e.g.*, the CPU) to another external device (*e.g.* system memory) because of differences in rates of data flow or time of occurrence of events.	storing data temporarily to compensate for differences in rates of data flow, time of occurrence of events, or amounts of data that can be handled by the devices or processes involved in the transfer or use of data

ProMOS, again, has impermissibly and completely avoided the specification to construe

the "buffering" claim term. Instead, ProMOS again relies solely on a dictionary to attempt to construed this term out of the context of Chan's invention, violating *Phillips*, 415 F.3d at 1313.

Freescale's construction of "buffering", on the other hand, is based on the meaning of claim terms within the context of the patent. (DI 85, at 45.) Chan defined "buffering" as occurring between two external devices through consistent use in his specification, and Chan's (and Freescale's) definition therefore should be adopted. *Bell Atl.*, 262 F.3d at 1268.

D. "selectively providing" - '709 Claims 1, 13, 17 and 22

Freescale	ProMOS
providing data held in a register depending on certain conditions and never providing the data held depending on other conditions	Does not need construction. To the extent the Court decides to construe the term anyway, it means: providing on a selective basis.

ProMOS has chosen not to propose any construction for this claim term (other than in the alternative to circularly shuffle the claim terms around), presumably to permit it to later twist the meaning of this term to suit its particular infringement needs. For the same reasons provided above and at DI 85, pp. 47-48, ProMOS's position should be rejected and Freescale's proposed construction of "selectively providing" should be adopted.

E. "selectively providing the first data to one of said random access memory, said system port, and said random access memory and said system port" - '709 Claim 1

Freescale	ProMOS
The selectively providing claim phrase means providing the first data to: [a] said random access memory and not to said system port under one set of conditions, [b] said system port and not to said random access memory under a second set of conditions, and [c] said random access memory and said system port under a third set of conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" above, and ProMOS's position on "selectively providing" and "random access memory above.

ProMOS has also chosen to not propose a construction for this claim phrase either, again presumably to maximize its flexibility later. For the same reasons provided above and those provided at DI 85, pp. 47-48, Freescale's proposed construction of should be adopted.

F. "at the same time" - '709 Claim 13 and 22

"wherein the input data *is provided* to said random access memory from said memory write register *at the same time* that the output data *is provided* by said write back register to said system port" (709:13)	
Freescale	**ProMOS**
whenever input data is provided to the RAM, output data must be provided to the system port	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "is provided" and "at the same time" need to be construed, these terms are clear on their face.

ProMOS has, again, chosen to not propose a construction for this claim phrase, presumably for the same purposes discussed above. Despite claiming that "at the same time" need not be construed, ProMOS, nevertheless, argues that Freescale's construction is wrong. As an initial matter, ProMOS's criticism confirms the need to construe this term because there is an obvious disagreement. Moreover, ProMOS's contention--that Event A may, but need not always, occur when Event B occurs--turns the explicit claim language that each event "is provided . . . at the same time" on its face. The inventor could just have easily drafted, but chose not to draft (because it was not his invention), language to claim that "Event A and Event B have to happen at the same time at least some of the time." Chan, however, did not use such qualifying language, and instead purposefully and explicitly claimed that both events always had to happen at the same time. For these reasons, Freescale's construction should be adopted.

III. TERMS IN WHICH PROMOS'S GOAL IS TO AVOID CONFRONTING INDEFINITENESS ISSUES

A. "register" terms

"host input register" - Chan '241: 10, 15	"first input register" - Chan '241: 16
"system output register" - Chan '241: 10	first output register" - Chan '241: 16
"second output register" - Chan '241: 16	system input register" - Chan '241: 10, 15
"second input register" - Chan '241: 16	

Similar to the "bus" terms, instead of addressing the complete "register" terms Freescale identified for construction, ProMOS has chosen to only construe the word "register". In other words, ProMOS is impermissibly reading out the qualifying and descriptive adjectives the inventor intentionally chose to use to claim his various "register" terms and, in the process,

attemps to avoid the various problems caused by those other claim words, which, by law, cannot be superfluous and must have some meaning attributed to them.[27]

Moreover, despite the fact that the term "register" appears 369 times in the Chan specification, ProMOS provides no intrinsic support for its construction. ProMOS would obviously prefer to construe "register" in the abstract, and thereby avoid construing the various other register terms in the context of the specification, another approach expressly rejected by the Federal Circuit. *See Phillips*, 415 F.3d at 1313-17.

ProMOS adopted this approach because the fully-claimed "register" terms are neither defined, nor even mentioned, in the specification. Because these register terms have no ordinary meaning and were simply invented for inclusion in the claims after the initial Chan patent applications were filed, one of ordinary skill in the art would not be able to determine their meaning from the intrinsic evidence and the terms are therefore fatally and insolubly indefinite. Chan's failure to provide any guidance in the specification as to meaning of these register terms makes it impossible to ascertain the scope of the claims that contain them. For the reasons set forth herein and in Freescale's opening brief, these claim terms should be found indefinite.[28]

B. "operably decoupled" - '241 claim 1

Despite admitting--as it had to--that "operably decoupled" is not a commonly understood term, ProMOS nevertheless argues that no construction is required. (*See* DI 84 at 22.) Indeed,

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[27] *See Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1119 (Fed. Cir. 2004) ("Furthermore, we observe that . . . interpretation largely reads the terms 'operatively' out of the phrase 'operatively connected' . . . [rendering] the term 'operatively' . . . unnecessary and superfluous as the patentee could have as easily used the term 'connected' alone.").

[28] *See, e.g., Honeywell Int'l, Inc. v. Int'l Trade Comm'n*, 341 F.3d 1332, 1339-41 (Fed. Cir. 2003) (holding the claims "insolubly ambiguous" because the specification and prosecution history gave no guidance as to what one of ordinary skill would interpret the claim to require).

ProMOS has to take this position because it cannot offer any meaningful construction of this indefinite term. As demonstrated in Freescale's opening brief (DI 85 at 51-52), Chan also used the claim term "decoupled" throughout the claims. How can "decoupled" and "operably decoupled" possibly mean different things; for example, when "decoupled" is used by itself, does it mean the nonsensical "inoperably decoupled"? Of course not, and yet the law requires that "operably"--a term intentionally included at certain times by the inventor--be given some meaning and not simply read out of the explicit claim language. *See Innova/Pure Water,* 381 F.3d at 1119. The bottom line is that "operably decoupled" is not sufficiently precise to put the public on notice of the boundaries of the asserted claims' scope because the term was invented by Chan for purposes of its patents, but is not defined anywhere in the original disclosure. "Operably decoupled" therefore renders any claim containing the term fatally indefinite.[29]

C. "operations at said system port to be decoupled from said random access memory" - '709 claims 17 and 22

For this claim phrase, ProMOS has also chosen not propose a construction, presumably (once again) to preserve its ability to flexibly apply this phrase later to suit its particular infringement needs and to avoid indefiniteness issues. Again, ProMOS's claim construction strategy should be rejected for the reasons provided above.

It is perfectly understandable why ProMOS would not want this claim phrase construed. The claim phrase is internally inconsistent when read in the context of the specification and is therefore indefinite. Claims 17 and 22, recite that "the holding and selective furnishing of the first output data [by the write back register] and the holding and selective providing of the second input data [by the memory update register] allows write back and memory update operations at said system port to be decoupled from said random access memory." ('709 at

[29] *See, e.g., Morton Int'l. Inc. v. Cardinal Chem. Co.,* 5 F.3d 1464,1470 (Fed. Cir. 1993).

76:18-55; 77:5-78:5.) The memory update operation involves providing the second input data to the random access memory. The memory update operation therefore cannot be decoupled from the random access memory if it is providing data to the random access memory.

D. "buffering and selective provision of data to and from said cache storage locations by said plurality of registers" - 241 claim 1

ProMOS, again, has chosen not to propose a construction, which is understandable. The claim phrase is not enabled by the Chan specification, and is also inconsistent with Chan's use of the term "buffering" in the specification. In particular, the function of "buffering and selective provision of data *from* said cache storage locations" is inconsistent with the Chan's definition of "buffering" which involves using a storage element (*e.g.*, memory write register) as an intermediary device to hold data temporarily while the data is waiting to be transferred from one external device (*e.g.*, the CPU) to another external device (*e.g.* system memory) because of differences in rates of data flow or time of occurrence of events. For the reasons provided in Freescale's opening brief at 54, the claim phrase "buffering and selective provision of data to and from said cache storage locations by said plurality of registers" should be held indefinite.

E. Indefinite Means-Plus-Function Terms

ProMOS has made up structure out of whole cloth (because it is not disclosed in the specification as required) in an effort to save these indefinite means-plus-function clauses.

1. Presumptive means-plus-function terms

- means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the second data held in said write back register for write back to said system port (Chan 709:10)
- means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back register for write back to said system port (Chan 709: 26)

Freescale agrees that the function identified by ProMOS for these means-plus-function phrases are the correct functions. The dispute here, however, is whether ProMOS has identified

structure that is clearly linked in the specification to the performance of the function. This duty to clearly link or associate structure to the claimed function is the *quid pro quo* for the convenience of employing § 112 ¶ 6. *Budde v. Harley-Davidson, Inc*., 250 F.3d 1369, 1377-78 (Fed. Cir. 2001). Structure that is not specifically linked to the claimed function cannot be corresponding structure under 35 U.S.C. § 112 ¶ 6, even if that structure is known to one of ordinary skill in the art. *See Atmel Corp. v. Info. Storage Devices. Inc*., 198 F.3d 1374, 1380 (Fed. Cir. 1999) (finding that "consideration of the understanding of one skilled in the art in no way relieves the patentee of adequately disclosing sufficient structure in the specification").

As demonstrated at pp. 49-50 of Freescale's opening brief, the patent specification fails to identify *any* structure that actually performs the specified function of "identifying ones of the fetched data…" Implicitly acknowledging this fatal deficiency, ProMOS argues that the "valid bits" are the required structure. However, a "bit" merely contains a value; it does not perform a function. To the contrary, some structure (undisclosed in the Chan patent) will interpret the value of that bit and perform some function based on that value, but it is not the bit itself that performs the function. ProMOS's sole support for its construction is a statement that "Valid bits make partial write of fetched lines possible." (DI 84 at 19.) This quote does not (because it cannot) state that the "valid bits" actually perform a function. The critical question is what *structure* uses those valid bits to perform the specified function; that the valid bits purportedly are used by that unspecified *structure* is irrelevant. Because the patent specification fails to link definite structure to the performance of the identifying function, the claims containing these means-plus-function terms are indefinite.

- means for masking the providing of selected ones of said words of the fetched data to said random access memory (Chan 709: 12)
- means for masking writing of selected words of the system fetch data into said random access memory (Chan 709: 21, 24)

- means for masking writing of selected words of data into said random access memory (Chan 241: 26)

Similarly, Freescale agrees that ProMOS has identified the correct functions for these phrases. Once again, however, ProMOS has not (because it cannot) identify any *structure* that is clearly linked in the specification to perform those claimed functions.

For the same reasons discussed above with respect to valid bits, the "mask bits" identified by ProMOS here are not structure that performs the masking function. Once again, the patent specification fails to identify the structure that uses those mask bits to actually perform the function. As discussed above, a bit is merely an indicator; it does not and cannot perform *any* function. Some undisclosed structure interprets the bit and performs some function, but that structure is not the bit itself. Because the patent specification fails to link definite structure to the identifying function, the claims containing these means-plus-function terms are indefinite.

- means for disabling said dual port cache memory during a local bus access cycle (Chan 241: 5, 19)

This phrase is indefinite because ProMOS has not pointed to any "clear linking" in the specification of any structure to the identified function of "disabling said dual port cache memory during a local bus access cycle." The portion of the specification on which ProMOS relies (DI 84 at 21) says nothing about "disabling the dual port cache memory" during a local bus access cycle, let alone "clearly linking" any disclosed structure to performing that function; indeed, ProMOS does not even bother to try to (because it cannot) explain how the specification portions they cite have anything to do with disabling the dual port cache memory.[30] Moreover,

[30] ProMOS's citation of Table VI at column 39 merely states that there are no cache operations. It does not state that the cache has been disabled or that the controller disabled the cache. ProMOS's citations at columns 42:58-43:42 state that the cache controller does not pass local bus cycles to the system and that the cache controller does not make a cache hit/miss determination. Again, the citation does not state that the cache is disabled, as it is concerned (Continued . . .)

ProMOS has not identified corresponding structure that is clearly linked to the function recited in the claim. Instead, ProMOS merely picked a box on Fig. 33 and argued, without benefit of support, that "circuitry" in that box performed the required function. ProMOS could have just as easily chosen any other box in Figure 33 or the 486 CPU or even the dual port burst memory 72 in Figure 32 for that matter. ProMOS cannot meet its burden by just pointing to any structure it can find in the specification and then contending that such structure performs the identified function. "A structure disclosed in the specification qualifies as 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Default Proof Credit Card Sys. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). If the patentee fails to (a) adequately disclose and (b) clearly link the corresponding structure, that claim is invalid due to a failure to particularly point out and distinctly claim the invention as required by the second paragraph of § 112. *Biomedino, LLC v. Waters Techs. Corp.*, 490 F.3d 946, 948 (Fed. Cir. 2007). This duty to clearly link or associate structure to the claimed function is the *quid pro quo* for the convenience of employing § 112 ¶ 6. *Budde*, 250 F.3d at 1377-78. The Chan specification does not clearly link or associate structure to the claimed function and thus the claims containing this means plus function phrase should be held indefinite and, hence, invalid.

2. Non-presumptive means-plus-function terms

- first control sequencer for controlling addressing and data signals on said host address bus and on said host data bus (Chan 241: 4, 18)
- a second control sequencer for controlling addressing and data signals on said system address bus and on said system data bus (Chan 241: 4, 18)

The parties disagree regarding whether 35 U.S.C. § 112 ¶ 6 is applicable to these claim

(. . . continued)
only with cache controller operation.

terms. "When the word 'means' is not used in a claim term, a rebuttable presumption arises that § 112 ¶ 6 does not apply. This presumption can be rebutted, if the party advancing a means-plus-function construction demonstrates that the claim term fails to recite sufficiently definite structure or recites a function without reciting a sufficient structure for performing that function." *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 422 F. Supp. 2d 446, 459 (D. Del. 2006). In this case, the presumption should be rebutted because one skilled in the art would not know the precise structure for either a first or second control sequencer. Indeed, the functions of controlling addressing and data signals on the host and system data and address buses can be achieved using a variety of structures, such as (i) discrete logic gates; (ii) a state machine consisting of flip-flop elements, discrete logic gates, and feedback paths; (iii) a programmable logic array; (iv) a read-only memory; and (v) a microprocessor operating from a stored program. It is unclear what the specific structures are for performing the recited functions. Moreover, Chan did not describe any structure for performing the functions recited in these means-plus-function claim limitations and obviously did not clearly link or associate specific structure for the functions. There is no "corresponding" structure, and the claims are invalid under § 112 ¶ 2.

CONCLUSION

For all the reasons discussed in Freescale's opening brief and above, the Court is respectfully requested to not allow ProMOS to obtain claim coverage far beyond what the inventor Chan described and claimed as his invention throughout the intrinsic record and, instead, to adopt Freescale's proposed constructions for the claim terms in dispute.

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Dated: November 20, 2007
1316044

CERTIFICATE OF SERVICE

I hereby certify that on November 20, 2007, I caused the foregoing to be electronically filed with the Clerk of the Court using CM/ECF which will send electronic notification of such filing to the following:

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Additionally, I hereby certify that true and correct copies of the foregoing were caused to be served on November 20, 2007 upon the following individuals in the manner indicated:

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EXHIBIT K

Thin film deposition with physical vapor deposition and related technologies

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(Received 9 June 2003; accepted 17 June 2003; published 2 September 2003)

The properties of thin films depend critically on how they are made. For the most part, thin films are assembled in ways very different from the production of bulk materials. Thin films are usually deposited on existing, bulk surfaces using techniques based on atomic or molecular scale physics and chemistry. Physical vapor deposition (PVD) of thin films relies on the removal of atoms from a solid or a liquid by energetic means, and the subsequent deposition of those atoms on a nearby surface. Variations of PVD processes include thermal evaporation, physical sputtering, laser ablation, and arc-based emission. Additional modifications to physical sputter deposition have been made to enhance the chemical and/or structural nature of the deposited films. These modifications include reactive sputter deposition, the unbalanced magnetron, collimated and ionized sputter deposition. Each of these systems and techniques will be described as well as some of the current day applications of the films produced.
[DOI: 10.1116/1.1600450]

I. INTRODUCTION

Over the past century, thin films have become an intrinsic part of everyday life. The visible applications are wide-ranging across many fields; from microelectronics to automobile parts, and from windows on skyscrapers to the metallic coatings on the insides of bags of potato chips. The properties of thin films often differ radically from simply a thinner version of what we would call bulk material. As a simple example, the optical properties of thin dielectric film layers can be tuned by adjusting their thicknesses to transmit or absorb light at very specific wavelengths (or colors), and this is quite different from the behavior of the macroscopic or bulk glasses we are familiar with.

Thin film applications depend strongly on the electrical, optical, and physical properties of the materials chosen. These properties depend, in turn, strongly on the techniques and processes used to fabricate the films. The same deposition tool and technique used, for example, to deposit a clear, dielectric film with excellent optical properties can, with small changes in the parameters, result in opaque, metallic films more suitable for electrical conduction than optical applications.

The development of thin film deposition tools and techniques has spanned the entire 20th century and even extends back to the 1850s. In the early 1900s, thin film techniques were widely used for optical applications, such as mirrors for telescopes. By the middle of the century, films were becoming widely used for their physical properties, such as hardness and wear resistance. In the latter part of the 1900s, numerous applications developed for thin films, driven in large part by the development of the microelectronics industry, which itself is based almost entirely on the deposition and manipulation of thin metal, nitride, and dielectric films. Much of this latter work has been described in JVST, sometimes directly in the form of papers on thin film developments, and sometimes indirectly in that thin films and film deposition are simply an inherent part of some larger project or measurement.

This article attempts to describe the general tools and techniques used to make thin films. The tools are based on evaporation or sputtering (physical vapor deposition, or PVD), and many permutations have been found allowing deposition in wide-ranging and unusual cases. The article will describe PVD processes first, followed by innovations to the basic processes and techniques which allow greater control over the microstructure and/or the stoichiometry of the film, as well as the ability to coat unusual topographies on surfaces.

II. PHYSICAL VAPOR DEPOSITION OF THIN FILMS

Physical vapor deposition, or PVD, covers a range of thin film deposition techniques which include evaporation, laser ablation-deposition, vacuum-arc based deposition, and many different modes of physical sputter deposition. While the current-day usage of the term PVD has often been focused on just sputter deposition from magnetron sources, a description of these other processes can help broaden the understanding of both the generation process of the depositing atoms as well as the deposition process at some sort of sample or electrode.

PVD processes generically involve individual atoms or perhaps small clusters of atoms which are not normally found in the gas phase. Typically these atoms are removed from a solid or liquid source, transit an evacuated chamber, and impinge on a solid surface at which point the atoms stick and form a film. The means to remove the atoms from the original source can be by thermal heating of the source or energetic particle bombardment by electrons, atoms, ions, molecules, or photons. The removal process can be thermodynamic, as is the case typically with evaporation and ablation, or may be the result of a sequence of energetic colli-

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sions near the surface which results in the kinetic ejection of atoms from the source; a process generically called sputtering.

Once the atoms or small atom clusters are removed from the original surface, they diffuse within an evacuated chamber until they impinge on a solid surface, at which point there is a probability for condensation. Since this paper is focused mostly on thin film deposition, this description will not be extended to cases where the deposition surface is hot enough that the deposition atoms re-evaporate, although elevated surface temperature may lead to changes in film structure or stoichiometry. There will also be relevant cases where the depositing surface undergoes energetic bombardment during deposition which can result in ejection or sputtering (often called re-sputtering) of the depositing atoms. The most common example of this is known as bias sputtering, where the depositing film sample is located on a biasable electrode and receives energetic bombardment from the plasma in the chamber or a separate ion or neutral beam source.

PVD differs from chemical vapor deposition in that the primary source of the depositing species is a solid or liquid, as opposed to a gas, and has a vapor pressure much below the working pressure of the deposition system. However, chemical reactions can and do occur in PVD systems, virtually always at the depositing film surface. This could be as mundane as the incorporation of residual gases from the vacuum system into the depositing PVD films. Alternatively, a reactive gas species (such as oxygen or nitrogen, for example) can be included in the chamber during deposition to intentionally be included in the film in the form of an oxide or nitride. The presence of the reactive gas in the chamber, however, can significantly alter the PVD source as well, so the system must be well understood.

A. Evaporation: (a) Sources

Evaporative sources fall into two general classes; quasiequilibrium and nonequilibrium,[1] both of which are used widely for different applications. In the quasiequilibrium source, the evaporation process occurs in a nearly steady state equilibrium with its vapor. An example of this type of source is the effusion or Knudson cell (Fig. 1), which is generally a heated, closed container with a fairly small orifice. If this orifice is small compared to the remaining interior surface area of the cell, losses through the aperture are mostly a perturbation on the dynamics of the liquid-vapor equilibrium in the cell.

The nonequilibrium evaporation source can be characterized as an open source, where a small region of liquid material evaporates off into a large, low pressure volume. Since the pressure in the region of this liquid source is low, there is no return or equilibrium of the evaporated vapor flux to the source. Examples of this type of open source are the boat, the crucible, and the e-beam source [Figs. 2(a), 2(b), and 2(c)]. The boat source is typically constructed of a refractory metal, such as W or Ta, which is then heated by passing a large current through the band of metal forming the boat. The crucible source is often a ceramic cup wrapped with a coil of metal wire which is resistively heated by passing a large

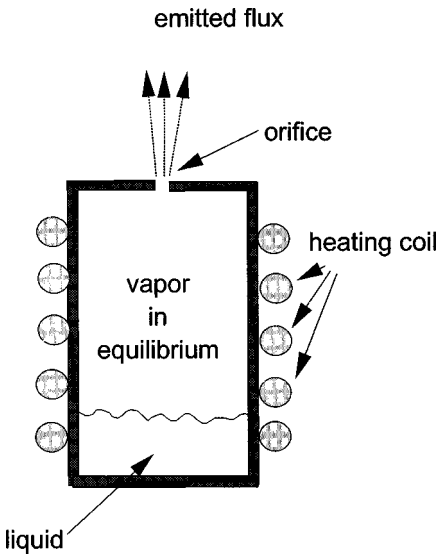

FIG. 1. Schematic of a Knudson or effusion evaporative source.

current through the wire. The e-beam source, which is perhaps most commonly used, uses an energetic electron beam which originates from a filament at location underneath or adjacent to the evaporation point. The path of the emitted electrons is bent by a static magnetic field such that the filament is not in the line-of-sight of the evaporation point. The kinetic energy of the electron beam heats up an open crucible of material to the melting point and beyond.

In the boat or crucible sources, the evaporant material is usually completely melted, and this may lead to chemical interactions between the evaporant species and whatever the boat or crucible is made of. Mahan[1] describes the three ''laws'' of high temperature chemistry, attributed to Spear;[2] (a) ''at high temperature, everything reacts with everything,'' (b) ''the higher the temperature, the more seriously everything reacts with everything else,'' and (c) ''the products might be anything.'' While the boats are typically refractory materials, and the crucibles typically ceramics, the nature of the reactions is such that these sources are only appropriate for very low temperature evaporations.

The e-beam source cleverly avoids this problem by making a self-forming ''crucible'' of the evaporant material out of itself. The material to be evaporated is placed into an open metal cup which is water-cooled. The incident e-beam has sufficient energy to melt a relatively small spot on the top of this material. This small area of liquid is heated well above the melting point at the surface, but the temperature at the bottom of the liquid is much colder, such that the adjacent material does not even reach the melting point. Therefore, the molten metal is only in contact with a de-facto crucible made of the same material, and hence any chemical reactions with contaminants are eliminated.

Evaporative deposition occurs simply by placing a sample in the direct line-of-sight of the source. Typically, there is a modest distance between the source and sample (10–100 cm) for the practical reasons of allowing a larger deposition area and to limit sample heating by optical radiation from the

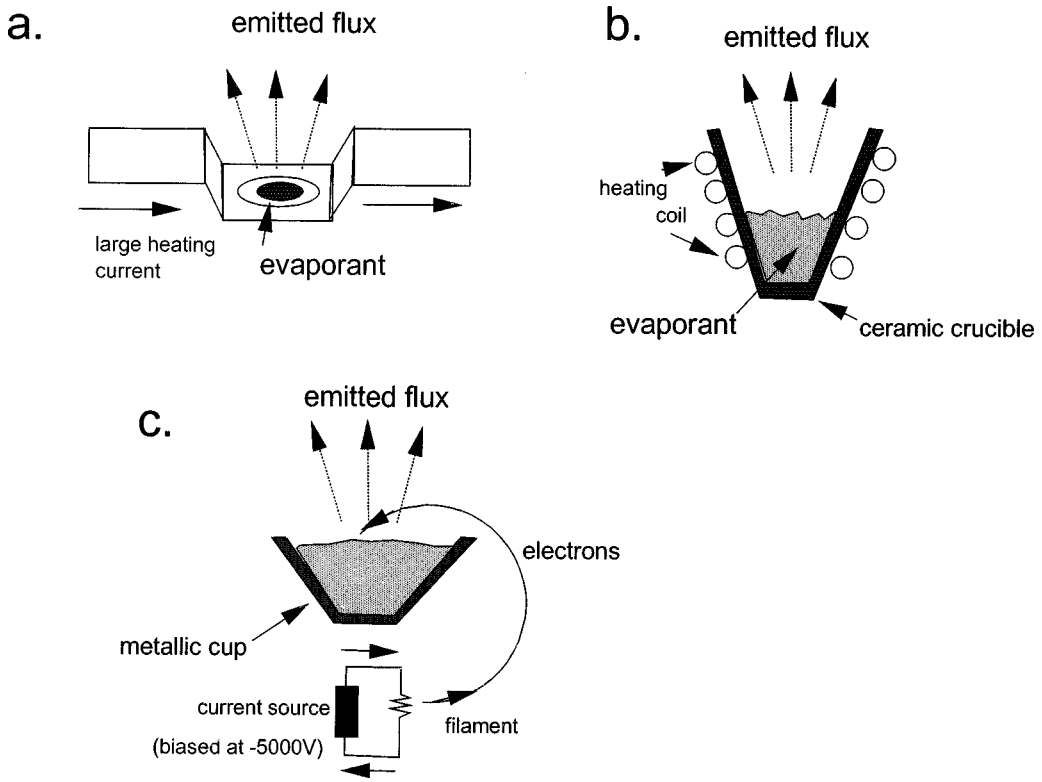

FIG. 2. (a) Boat evaporative source, (b) crucible source, (c) e-beam source.

source. The flux is emitted from the source with roughly a cosine distribution and the deposition rate at the sample scales as roughly the inverse of the distance squared. Since the evaporated flux in many sources can be significant (microns/minute at short distances), it is possible to deposit on a fairly large area at a reasonable rate (100 nm/min). Evaporative systems are often configured with a parabolic dome onto which many samples are attached. A large evaporator might have a dome diameter of over a meter and hold 25 or more than 125 mm substrates, or perhaps 10–12 200 mm substrates.

Evaporation has also been used on a much larger scale for such things as the deposition of mirror coatings on large telescope reflectors (many meters in diameter), depositions on windows used for large buildings, and also on rolls of plastic film, which might be 2 m wide and many miles in length. The latter case shows up as the metallic inside coatings on bags of potato chips or other food packaging.

Most evaporative deposition systems require low vacuums to operate efficiently. Aside from the issue of impurity incorporation discussed in a later section, it is desired that the mean free path of the evaporant flux exceed the distance to the sample. This reduces in-flight scattering with the background gas, which can lead to reduced deposition rates. A rough relationship between pressure and mean-free-path is that the path length is 5 cm at 1 mTorr of pressure, and scales inversely with pressure. Therefore, the maximum pressure for an evaporative deposition with a sample distance of 1 m would be 10^{-5} Torr. At pressures much above that point, the deposition rate will drop due to in-flight gas scattering of the evaporated atoms.

B. Evaporation: (b) Alloys

Evaporation as a deposition technology suffers from two major limitations. The first is that it is a near equilibrium deposition process. That means at the film surface, the evaporated metal atoms arrive thermally and condense in thermal equilibrium with the surface. Since this surface is typically much colder than the source temperature, a thin film is usually deposited. However, the film material is subject to issues related to wetting, nucleation and cluster formation, and agglomeration, which may result in less-than-ideal film properties. This will differ significantly from the case of physical sputter deposition to be discussed in the following, where the depositing atoms arrive with significant kinetic energy and more nearly implant themselves onto the surface.

The second major constraint with evaporation-based deposition is the difficulty in evaporating and forming alloy films. Since each atomic species has a different temperature–vapor pressure relation, (Fig. 3), the evaporation rate of two different materials in a common crucible or source is very different. Typically, the lower melting point or higher vapor pressure component material will evaporate first leaving behind the higher melting point or lower vapor pressure material. At the film surface, therefore, the initial depositing flux will be of the low melting point or higher vapor pressure

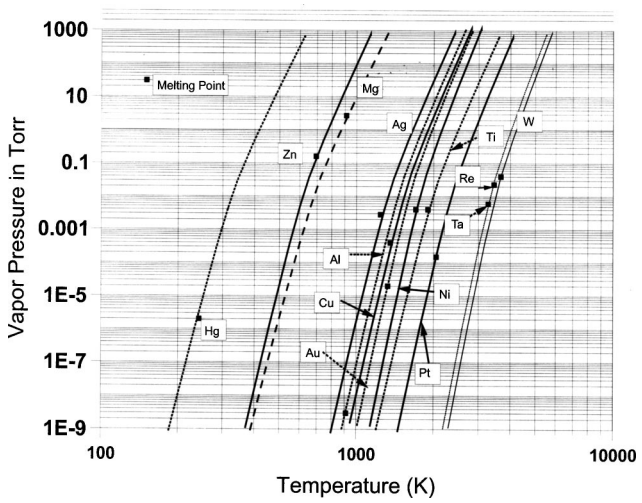

FIG. 3. Vapor pressure vs temperature plots for many elements (adapted from Hoenig, RCA—Ref. 3).

material with perhaps a low concentration of the higher melting point species. After the first material is exhausted from the source, the film deposition will then transfer to the higher melting point material.

The only practical solution to this problem is to have two adjacent sources, one for each material, and adjust the emission rates to the desired level. This is known as coevaporation. An experimental constraint of this approach is that the usual control mechanism for evaporation is to use a quartz crystal microbalance exposed to the depositing vapor at a location near that of the sample. With multiple evaporation sources, it is necessary to place a tube-like collimator over the rate monitor surface to constrain its deposition to only a single source. A second experimental issue for coevaporation is that due to the distance between the two (or more) evaporation sources, the deposition rate of each component will vary spatially around the chamber. If the sample position is fixed, the relative alloy composition can vary across the sample surface because one side of the sample will be closer to one of the sources than the other. While this can be a useful research technique for making many samples of differing composition in a single deposition, it limits the useful size of a controlled composition deposition. Practical solutions to this problem are to move the sample location very far away from the source, or else to provide some means of sample motion (rotation or planetary) to average out the distance from the sample to each source.

However, a disadvantage from one point of view can be an opportunity from another. In the case of deposition from two separate evaporation sources, there will be a relative composition change as a function of the distance from each point. Since the deposition rate falls roughly as $1/d^2$, where d is the distance from the source to the sample, a sample located closer to one source will receive a higher relative flux from that source than from the other. So, samples on one side of the chamber will be enriched in the material from the closest source, and samples on the other side will have the opposite enrichment. This allows for the deposition of many samples of different composition to be deposited with a single deposition run. This technique has been used numerous times to sample a wide range of chemical compositions to explore new materials, alloys, and compounds.

A second practical solution for alloy deposition is to heat the evaporation source very rapidly to a temperature well above the melting point of both materials and completely evaporate a small charge of material very rapidly, a technique known as flash evaporation.[4] This technique is limited to very small or thin depositions and may be easily contaminated by chemical reactions with the crucible, boat, or e-beam pocket.

For these rather mundane reasons, evaporation is rarely used for the deposition of alloy films in semiconductor manufacturing or nonresearch applications. As will be seen with sputtering (below), alloy deposition is conceptually much simpler, although it requires the investment of specific composition targets. Evaporation is widely used for the coating of architectural glass, large-area plastic sheets for food processing, and in some IC packaging applications.

C. Evaporation: (c) Reactive evaporation

Reactive evaporation is the formation of compound films composed of a species from an evaporation source and another species which arrive from the gas within the evaporation chamber. An obvious example of this is just the contamination of depositing films which can occur due to poor vacuum, in which oxygen, carbon, nitrogen, or water react with the depositing films to form usually unwanted, nonmetallic films. The relative arrival rates of the evaporated and background gas species can readily be calculated. If a deposition rate is desired of perhaps 50 nm (500 Å) per minute, the depositing flux needs to be approximately 3 atomic layers/s. At a base pressure of 10^{-6} Torr (usually water, C–O species, and hydrocarbons), the arrival rate of gas atoms or molecules to the surface is 1 monolayer/s. Therefore, if the evaporated species is very reactive (perhaps something like Al or Ti), a base pressure on 10^{-6} Torr might result in the deposition of a very nonmetallic, compound film of oxides, nitrides, and carbides. If the contamination rate was to be constrained to 1%, the base pressure would need to be 10^{-8} Torr or so. This requires good vacuum design and practice, particularly since many evaporators are large, batch systems with o-rings, lots of surface area, and only modest pumping. The other alternative is to increase the deposition rate by one to two orders of magnitude, if possible. There are other practical limits to this in that the evaporation source emits a lot if infrared heat within the vacuum chamber which can increase the functional base pressure during deposition sometimes several orders of magnitude by desorbing wall contamination.

It is also possible, however, to intentionally add reactive species to the evaporation chamber to form a compound thin film. The most common example of this is the addition of oxygen to a metal evaporation process to form a dielectric, oxide film. A wide range of materials will form oxides spontaneously on the depositing film surface if exposed to ad-

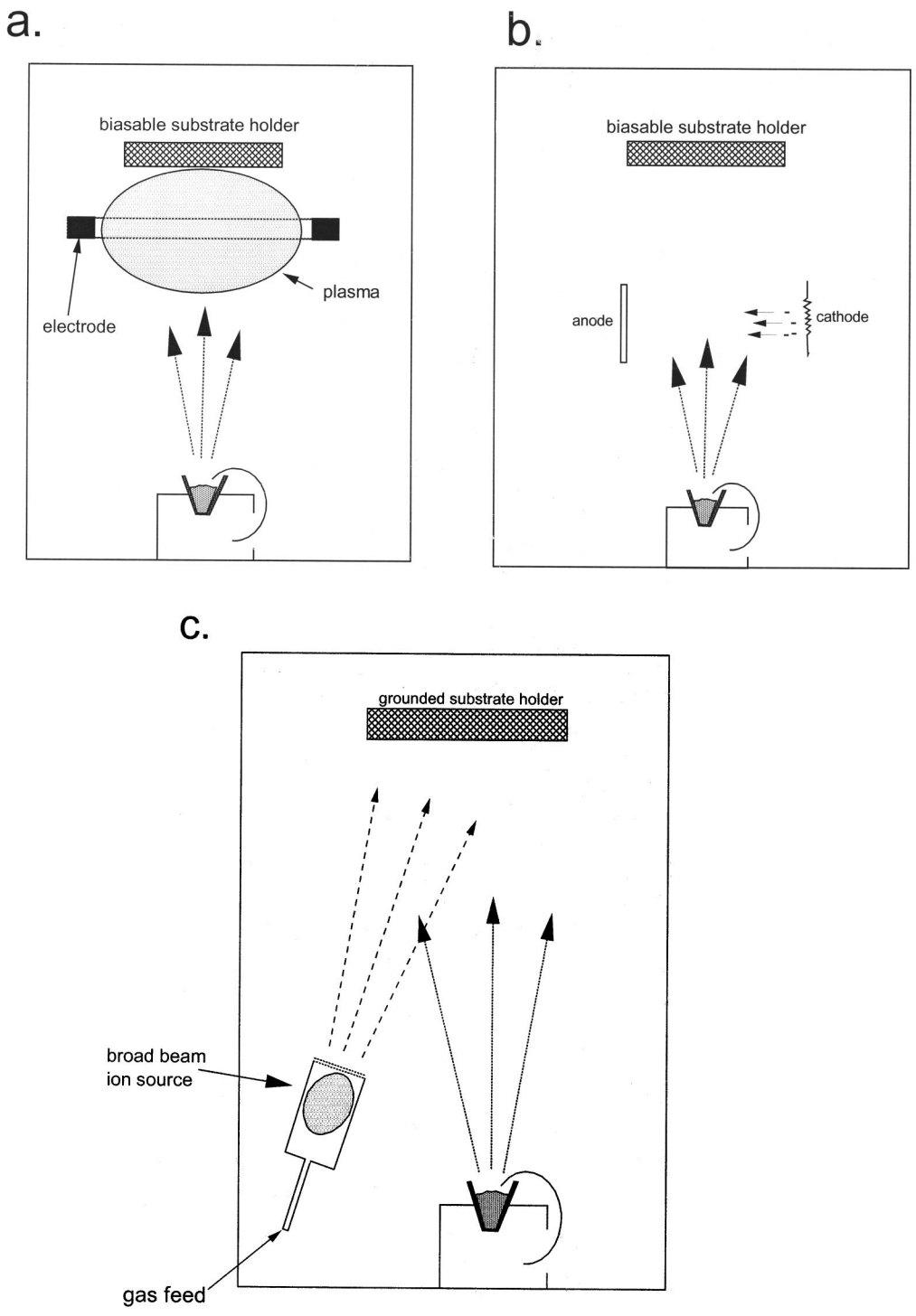

FIG. 4. (a) Activated reactive evaporation (ARE), (b) partially ionized beam (PIB), and (c) ion beam assisted deposition (IBAD).

equate oxygen during deposition.[5] This pressure need not be too high; typically in the 10^{-5} Torr range. Higher pressures can result in increased in-flight gas scattering of the depositing metal atoms and a reduced deposition rate.

A permutation on reactive deposition is the case where a plasma or some degree of ionization is used to alter the deposition process. Known by a number of terms, such as activated reactive evaporation,[6] partially ionized beam,[7] ion beam assisted deposition[8] [Figs. 4(a), 4(b), and 4(c)], and others, these are cases where ionization of either part of the depositing evaporant or gas flux, and subsequent acceleration of those ions to the depositing surface by means of a bias or in the form of an ion beam can result in increased reaction rates for the formation of compounds at the film surface. The bias results in increased incident energy for the ionized species, and this extra energy is then used to form compounds, typically nitrides, which would not form from neutral fluxes alone at the sample temperature.

D. Evaporation: (d) Other permutations; pulsed laser deposition and cathodic arc deposition

Evaporation-like deposition can also occur if the source material is impacted with either a dense photon beam or an electrical arc. The deposition induced by photons is known as pulsed laser deposition (PLD),[9] and typically uses an excimer laser in the ultraviolet such as a KrF laser at 248 nm. The pulse of light is mostly absorbed in the uppermost 100 nm or so of the surface, which can lead to rapid vaporization and ablation of the source material. The parameters of the pulsed laser beam are a pulse of 20–30 ns with a pulse energy of 0.5–0.8 J. An ideal aspect of PLD is that the source material can be a metallic solid, a powder, ceramic pellets, or even a liquid. This has led to the use of PLD for the deposition of materials such as the yittrium–barium–copper–oxide superconductors or other perovskites such as barium–strontium–titenate, and barium–zirconium–titenate, which are difficult to fabricate by either conventional evaporation or sputtering. A constraint of PLD is that the area of the photon beam is fairly small, so depositing on large areas is difficulty. Excimer lasers are also very power inefficient and can be somewhat complicated and unreliable. PLD is most often used for research purposes to explore new materials on a small scale.

Cathodic arc deposition (CAD)[10] is another evaporation-like process in which a very high current (hundreds of amperes) direct-current arc is struck on a metallic, cathode surface. As this arc interacts with the cathode surface, a very high power density exists at the contact point which can cause vaporization of the cathode material, some (or much) of which may be ionized as it passed out through the arc itself. In many CAD systems, the arc is moved or steered around on the cathode surface by means of a magnetic field. This increases the utilization of the cathode material and limits the possibility of burning through the cathode at any one point. Because of the somewhat violent nature of the arc–cathode interaction, CAD systems often emit tiny droplets of cathode material, called microparticles or ''spits.'' These macroscopic droplets (microns or more in diameter) will also land on the sample to form films, but this is an undesirable effect since the droplet-induced films will be underdense and bumpy. In some deposition tools, this problem is overcome by using magnetic fields to bend away the emitted cathode atoms, which are ionized in the arc, to a sample location out of the line-of-sight of the arc location.[11,12] The droplets, which are not ionized, will then deposit elsewhere in the system and not on the sample. This technology is known as filtered cathotic arc and has been used widely in manufacturing applications for the deposition of hard nitride coatings on tools, blades, turbines, and other metallic parts.

E. Sputtering and sputter deposition

Sputter-based processes differ fundamentally from evaporation in the kinetics of the particle emission process. In evaporation-based techniques, atoms are emitted thermally by heating a macroscopic region of the source material to the melting point and beyond. Sputtering can be characterized as a nonequilibrium process at the energy range of interest for film deposition. A sputtering event occurs when an energetic particle impacts a surface, which is also known as a target. The incident particle is usually an inert gas ion, but any ion, neutral atom, molecule, or even photon can be used if the energy is sufficient. The impact of the energetic particle on the surface kinetically dislodges one or more of the surface or near-surface atoms. These dislodged atoms, which have received considerable kinetic energy from the initial particle, move deeper into the target material and dislodge additional atoms. This process continues until the initial kinetic energy is spread among enough target atoms that the residual energy is insufficient to dislodge any more atoms, at which time the remaining energy is absorbed in phonons and this raises the local temperature. During this multiatom kinetic collision process, atoms near the surface may be dislodged with enough energy to overcome the surface binding energy and be emitted from the target. These atoms are known as sputtered atoms, and when they deposit on some other surface, the process is called sputter deposition.

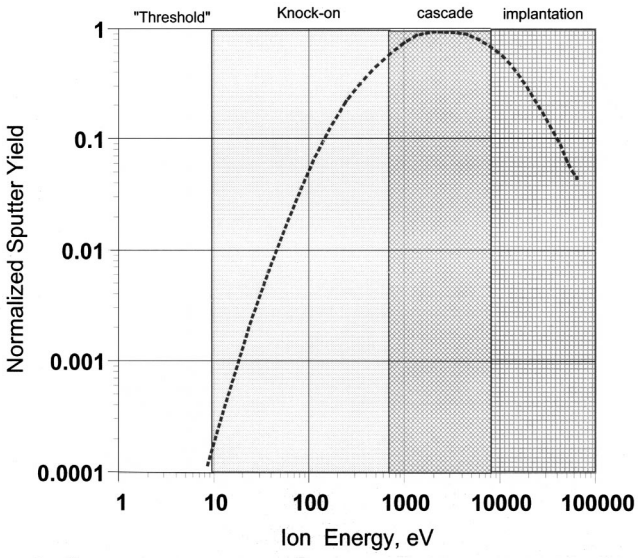

FIG. 5. Energy regimes of physical sputtering.

The mass and energy of the incident particle will determine many aspects of the resultant collision process (Fig. 5). At very low incident energies, there will not be sufficient energy to dislodge too many atoms. This was treated originally as a sputter threshold, and calculations were undertaken to predict the minimum possible particle energy that could result in an emitted, sputtered atom.[13] The concept of a sputter threshold was furthered by measurements of the sputter yield (yield=number of emitted atoms/incident particle) which plummeted at energies in the range of tens of electron volts. This concept of a sputter threshold was widely accepted (and is still widely accepted) until evidence became apparent with very high density plasma sources that sputtering was probably occurring at energies significantly below the classical threshold.[14,15] This was first observed (routinely) with electron cyclotron resonance plasma sources which were partially constructed of metallic areas as well as

dielectric areas. After operation at a kilowatt or so of microwave power into the plasma, metallic films were deposited on the dielectric surfaces in the source after several minutes. The plasma potential in these sources is readily measured at only a few volts but the ion currents are approximately 20 A/kW of incident microwave power. This suggests a sputter yield below 10^{-5} at a few electron volts, and this result is consistent with Monte Carlo modeling of sputtering at very low energies.[16]

At incident energies in the 50–2000 eV range, the sputtering process occurs roughly as described earlier; a somewhat random collision sequence near the impact point which may result in emission of near-surface atoms.[17] This range is called ''collisional'' or ''knock-on'' sputtering, and is the basis for essentially all thin film work. At higher energies (2–50 keV), the incident particle forms a collision cascade near the impact point which breaks all the bonds of a vast number of atoms and can numerically be treated almost as a very dense gas.[13] While this is an interesting theoretical and mathematical approach, and the explanations have been very convincing, this energy region is generally not used for film deposition and will not be covered further. At energies above 50 keV, the incident particle moves deeply into the target before depositing its energy. Since little energy is present near the surface, the sputter yields drop significantly, and the process is better described as implantation.

The energy and angular distribution of sputtered atoms differs significantly from evaporated atoms. Because of the energetic nature of the collision processes, sputtered atoms tend to have energies well exceeding the thermal energy that would be consistent with the source (or target) temperature.[18] The energy distribution of sputtered atoms has a peak at a few electron volts followed by a falloff scaling roughly as E^{-2}. The peak or average kinetic energy depends strongly on the mass of the sputtered atom as well as the energy and mass of the incident particle. Much of the original work on these energy measurements was done in the 1950s and 1960s by Wehner and colleagues using clever but fairly primitive means.[18,19] Other measurements, using more sophisticated means, have been made to refine the actual distribution of energies.[20]

The spatial distribution of the emitted, sputtered atoms is described generally as a cosine distribution. However, as a function of energy, this distribution can change into an under-cosine (usually lower ion energy), an over-cosine (higher incident energy), or can be somewhat more directional if the incident particle is inclined at a high angle to the surface. Usually the direction is opposite the incident direction and is called a forward-peaked distribution. For ion bombardment from a plasma, the incident ion direction is always at normal or near-normal incidence. However, for ion beam bombardment, the incident direction can be set by the geometry of the source and target.

F. Sputter deposition: Types of sources

Most practical applications of sputtering and sputter deposition are based on ion bombardment of the target surface. While bombardment by a neutral atom of the same mass will have essentially the same effect as an ion (since an ion is neutralized just before it hits the surface anyway), it is much easier to create large fluxes of energetic ions. Sputter deposition is typically practiced in either a plasma or an ion beam configuration. In the plasma systems, a cathode is used which is bombarded by ions from the plasma. If the energy and pressure conditions are appropriate, the cathode material is then sputtered off and can deposit on nearby surfaces. In an ion beam case, a beam of ions is generated using a remote source. This ion beam is then directed onto the target, and atoms are sputtered from the target onto a nearby sample. The parameter space for each process, as well as the applications and advantages of each will differ, but the underlying processes will be similar.

G. Plasma sources

A plasma can be generated under a variety of conditions, all of which result in the energetic removal of electrons from some of the gas atoms present in the volume under consideration. A plasma consists of three components; electrons, ions, and neutral species. In a processing plasma used for sputtering applications, the ion and electron densities are roughly equal, and one to three orders of magnitude lower than the neutral gas density. Plasmas used for thin film deposition are generated within vacuum systems usually by a voltage applied across an anode and a cathode within the chamber. In many cases, the anode is the chamber wall which is grounded and the cathode is then biased negatively. With the appropriate gas density and an adequate electric field between the anode and cathode, a plasma can be formed within the chamber. Since the plasma functions electrically as a conductor, its potential is constant spatially across the chamber and only changes significantly at either the cathode or anode (Fig. 6). Ions in the plasma which move near the cathode region can be accelerated at high energy to the cathode surface, and the bombardment of these ions onto the cathode can result in sputtering and emission of cathode atoms. Electrons in the plasma move toward the anode and only those energetic enough to overcome the slightly negative potential gradient at the anode are collected.

This type of plasma is called a diode, and is the basis for most PVD applications. The plasma is sustained by the emission of secondary electrons from the cathode surface caused by the ion bombardment. These electrons are quickly accelerated into the plasma by the large electric field present at the cathode. These energetic electrons are the energy source to the plasma and lead to additional ionization of gas atoms through two processes. The first is by means of electron–electron or electron–wave scattering which results in a general heating of the electron population in the plasma. The result is a Maxwellian-type electron energy distribution with a ''temperature'' in the electron volts range. Ionization then occurs by collisions between the electrons in the energetic tail of this distribution which have sufficient energy to ionize the gas atoms within the chamber. This is the dominant ionization process in all diode plasmas.

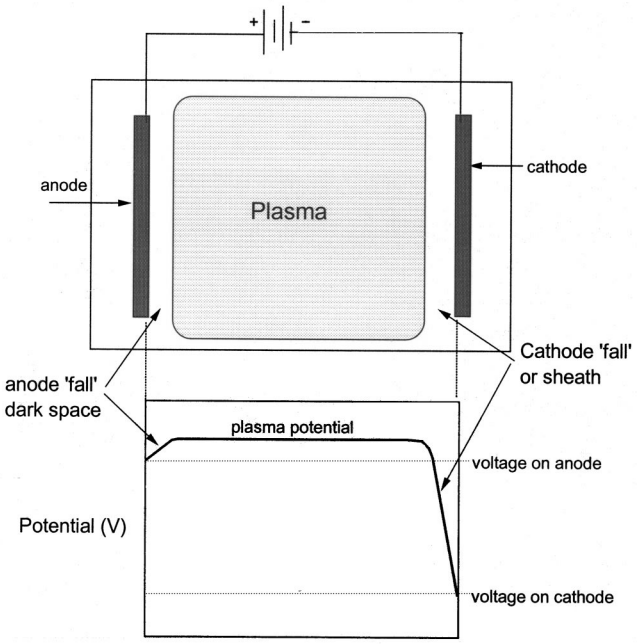

FIG. 6. Sketch of a simple diode plasma showing cathode, anode, and the relative potential as a function of position along the centerline of the plasma chamber.

A second process that also occurs in a diode plasma is the direct ionization of background gas atoms caused by a collision with an energetic secondary electron from the cathode. Secondary electrons are emitted from the cathode due to ion bombardment and are accelerated into the plasma across the cathode sheath, gaining many hundreds of electron volts of energy. Ionization of gas atoms by these energetic secondaries, often called ''primary ionization,'' actually occurs at a low rate compared to ionization by the Maxwellian electrons, because the number of secondaries is low and the cross section for ionization of most gases drops rapidly at high energy.[21] One continuing fallacy of the general, or public understanding of diode plasmas, is the role of direct or primary ionization by secondary electrons. This process is a minor component to the ionization processes needed to sustain a plasma. The dominant mechanism by far is ionization by the energetic tail of the Maxwellian distribution.

H. Plasma sources: dc and rf diodes

Diode plasmas have been known for well over 100 years and a broad range of operating characteristics has been understood and described.[22] Sputter deposition tools originally used dc diodes with an applied voltage of several kilovolts and current densities at the cathode in the 0.01 mA/cm^2 range. This type of deposition system was very inefficient because the energy of the secondary electrons was poorly utilized. At low pressure (mTorr), the plasma density was very low and most secondary electrons transited the plasma with few electron–electron, electron–wave, or electron–neutral collisions. In fact, most secondary electrons impacted directly on the anode (or sample) and caused heating but little else. If the chamber pressure was increased significantly (hundreds of mTorr), the coupling of the secondary electrons was more efficient and the plasma density was much higher. However, the transport of the sputtered atoms was greatly suppressed by in-flight gas collisions, and the deposition rate was reduced.

The underlying flaw with the dc diode was partially alleviated by the application of a rf voltage to the cathode and anode in place of a dc voltage. The applied frequency has mostly been set at 13.56 MHz, although significant work has been published at anywhere from a few kilohertz to 80 MHz or more. The use of a rf potential had two advantages. The first was that it facilitated the use of a dielectric target. Reactive sputter deposition will be described in the following, but it should be noted here that the sputtering of a metallic target in the presence of oxygen allowed the deposition of a dielectric film. But it also resulted in the formation of an insulating, dielectric surface on the cathode, which dramatically hindered the ion current to the cathode and virtually turned off the deposition process. By using a rf potential on the cathode, it was possible to sputter a dielectric target at a modest rate.

The second advantage of a rf diode is that the coupling of the energy from the electrons is better. Because of the oscillatory nature of the applied electric field, the electrons tended to be more readily retained in the plasma and their energy was increased by a wave-coupling process.[23] This resulted in a plasma density increase, compared to the equivalent dc case, and a higher likelihood of absorbing the kinetic energy of the secondary electrons in the plasma. While rf diodes still operate at potentials of 1000 V or more, the current density at the cathode increased to 0.1–0.5 mA/cm^2, which was a significant improvement over the dc diode. rf diodes require the use of high frequency matching networks to efficiently couple the power from the power supply into the plasma. These networks, which are usually automated with feedback loops to minimize reflected power, add considerable complexity to the tools.

Both dc and rf diodes can also function in a hollow cathode mode, which can be used to significantly increase the plasma density. The hollow cathode is a fairly simple device which uses geometry to reduce secondary electron losses. A hollow cathode has an open enough structure that the plasma penetrates into the cathode volume. This will occur whenever the width of the opening exceeds two to three times the Debye length, λ, which is a measure of the self-shielding of a plasma of the form:

$$\lambda = (kT_e\epsilon_0/ne^2)^{1/2},$$

where n is the plasma (or electron) density, T_e is the electron temperature, k is Boltzmann's constant, and e is the electron charge.

In the hollow cathode, secondary electrons are emitted at the cathode surface by ion bombardment and are accelerated by the cathode sheath into the plasma. However, after the secondaries cross the plasma region within the cathode, they see the very negative potential of the cathode on the opposite side which reflects the secondary electron back into the

plasma volume. This reflection process can occur many times, and the electron will slowly lose energy due to collisions and scattering events, resulting in a much higher probability of transferring the energy of the secondary electron into the plasma.

This hollow cathode process has also been extended to rf-diode technology by Horowitz and others,[24,25] and can be used in either a planar or multihole geometry. Hollow cathodes also occur somewhat naturally within plasma chambers in pump ports and other semienclosed cavities. This can be observed visually in a plasma chamber by a brightening of the plasma in a window, pump, or gas entry port. Since the effect is stronger as the gas density increases, this is a particular problem for the gas entry port in many tools, and it is necessary to use internal screens to limit the plasma entry into these apertures.

Hollow cathode diodes turn out to be no particular advantage for sputter deposition. At a given discharge power, the plasma density in a hollow cathode can be 3–10× greater than the planar diode case, and the voltage proportionately lower. However, two issues interfere with higher deposition rates. The first is the awkward geometry of the hollow cathode, which has most of the ion bombarded surfaces at 90° from a potential sample position. The second is the nominal power dependence of sputtering. In the 300–2000 eV range, many sputter yields are roughly linear with energy. The sputtering rate at a constant voltage (ion energy) is also linear with ion current or flux. So the sputtering rate, and effectively the sputter deposition rate, scale almost linearly with discharge power {flux(I) times energy(V)}. At constant power, a higher voltage, lower current discharge will have much the same deposition rate as a higher current, lower voltage discharge. This has limited hollow cathode plasma applications to cases of reactive etching or deposition, where the large flux is more important than changes in ion energy.

I. Plasma devices: Magnetrons

A solution to the intrinsic flaws of both dc and rf diodes is to add a magnetic field to the region near the cathode. This field alters the trajectories of the electrons, causing them to spiral around magnetic field lines, which increases their path length significantly. Somewhat like the hollow cathode effect, this partial trapping or localization of the electrons results in increased ionization and hence higher plasma density. A magnetron is a special case of magnetic plasma enhancement where the magnetic field is configured such that the $E\times B$ drift paths of the electrons (also known as the Hall effect) forms a closed loop. There are a number of geometries (Fig. 7), including planar, conical, cylindrical and hollow, which all are based on the same closed-loop effect.[26] The most common is the planar case, where a transverse B field is arranged across the cathode surface. The strength of this field is typically a few hundred gauss at the cathode surface. In the circular-planar geometry, the B field is radial and the closed-loop path is a broad, circular, co-axial band near the magnetron surface. In the rectangular-planar device, the B field is also tangential to the surface and configured to

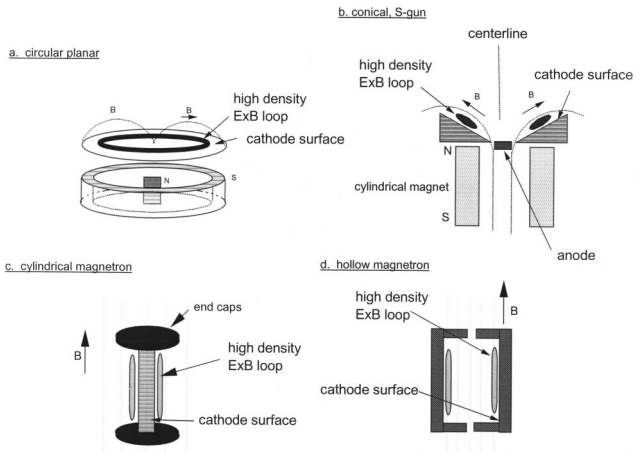

FIG. 7. Magnetron (diode) cathode geometries (planar, conical, cylindrical, hollow).

have a long, rectangular drift loop. Circular-planar cathodes tend to top out at diameters of 45–50 cm (used for 300 mm wafer deposition), while rectangular targets have been constructed which are many meters long.

The effect of this closed-loop trapping for electrons is to increase their effective path length in the near cathode region by two to three orders of magnitude, resulting in a much higher probability of collisions or scattering, and hence the transfer of energy to other electrons and to background gas atoms in the form of excitation and ionization. The plasma density in the drift loop can exceed $10^{12}\,\mathrm{cm}^{-3}$ even though the background pressure is just a few mTorr. The circulating current in the drift path can exceed the discharge current by 10× or more.[27] A magnetron cathode can operate at very high discharge currents, and current densities of tens to hundreds of $\mathrm{mA/cm}^2$ can be attained at discharge voltages of a few hundred volts.

The current voltage relationship of a magnetron has been characterized by an empirical relation of the form

$$I = kV^n,$$

where k is a system-dependent constant and the exponent n ranges from 5 to 100 or more. The empirical nature of this relationship has lead to much characterization and speculation about the nature of the discharge. It turns out that the exponent, n, depends on the sputter yield of the target, the secondary electron yield, the gas used, and may be related to gas rarefaction effects[28] driven by the transfer of kinetic energy from the sputtered atoms to the background gas,[29] an effect that was originally characterized by Hoffman as the ''sputtering wind.''[30]

Nevertheless, magnetrons function as nearly perfect diodes in that the discharge current can be increased almost indefinitely until the current limit of the power supply is reached or the target melts. Targets are water-cooled, but practical limits on water flow connections constrain cathode powers to $100\ \mathrm{W/cm}^2$.

Magnetrons tend to operate at pressures in the 0.5–30 mTorr range. At the lower end of this pressure range, the

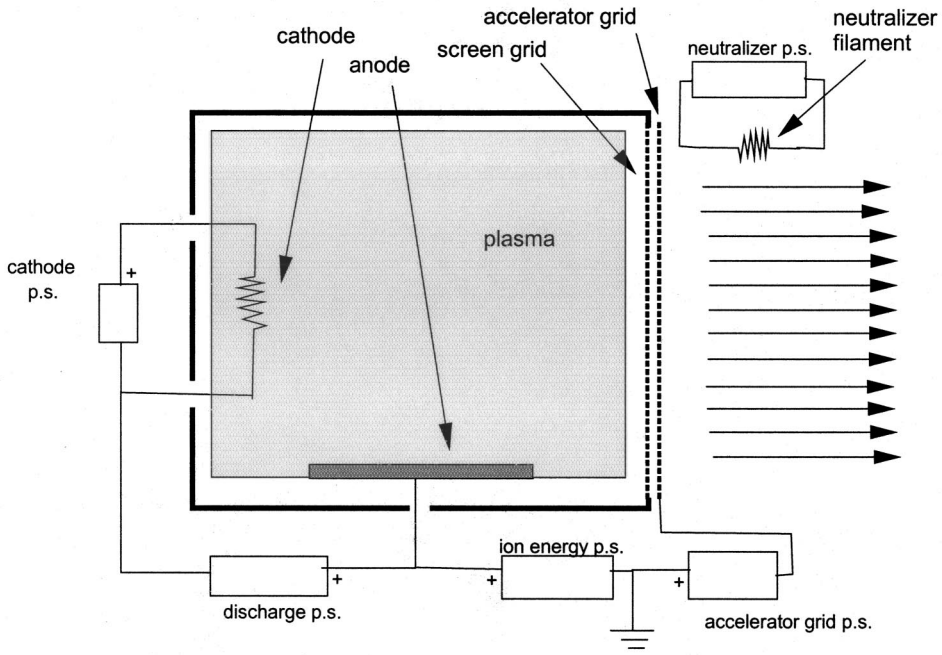

FIG. 8. Schematic of a Kaufman-type ion source.

mean free path for the sputtered atoms is 10–15 cm. At the upper end, the mean free path is 1 cm or less. At low pressures, the deposition is considered as line-of-sight, and this will have many implications on both the properties of the deposited films as well as the directionality of the depositing flux. At the upper end of the pressure range, the sputtered atoms lose all their initial kinetic energy from the sputtering process and are considered ''thermalized'' with the background gas. This will also alter the properties of the deposited films, and will be described below. At pressures above 30 mTorr (4 Pa), the magnetron will continue to operate but its effectiveness as a deposition source will be negligible due to the many in-flight scattering collisions of the background gas and the sputtered atoms. Descriptions of magnetron operation or properties at pressures higher than 30 mTorr are mostly academic in nature.

J. Ion beam sputtering and sputter deposition

In diode-based plasma devices used for sputter deposition, the sample generally sits exposed to the plasma which is used to sputter the target (cathode). This is geometrically limiting and also can subject the sample to undesirable heating or other forms of plasma-based damage. An alternative approach separates the plasma generation from the sputtering process, and uses a beam of ions from an ion source. These sources were originally developed as engines or ''thrusters'' for spacecraft, although many orders of magnitude more ion sources have been built for terrestrial applications. The general name for this type of source is a ''Kaufman Ion Source'' after the originator at NASA in the 1960s.

A Kaufman ion source consists of a plasma isolated and sustained in a closed volume.[31] The plasma is sustained by a dc or rf discharge. On one side of the closed volume are one to three grids or screens. Ions that impinge on the mostly open screens are accelerated by the voltages present and leave the source in the form of a broad beam (Fig. 8). The ion energy is set by the positive bias imposed on the plasma container, and might range from 300 to 2000 eV in practical cases. The ion current can be as high as a few mA/cm^2 at the higher energies, and the total beam power could be several hundred watts. Because of the positive bias of the source, the ions have energy with respect to ground, and thus can be used to sputter targets which are either grounded or unbiased. In the latter case, an electron-emitting filament called a ''neutralizer'' is used to limit charge buildup at the target being bombarded.

The beam is then directed through a vacuum chamber to a flat target, which is sputter-deposited onto the sample (Fig. 9). In this geometry and at an operational pressure of less than 0.1 mTorr, there are few gas-phase collisions of either the beam ions or the sputtered atoms, so everything is mostly

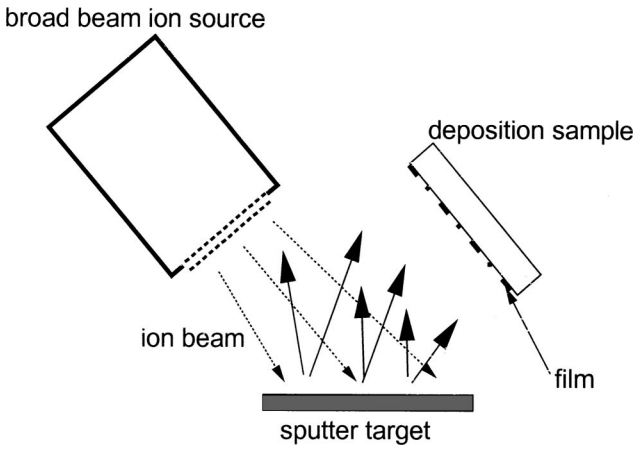

FIG. 9. Ion beam deposition system.

in a line-of-sight mode. The deposition rates with ion beam sputtering are usually much lower than with magnetron sputter deposition primarily because of the limited power density of the ion beam. There are some advantages, though. The target need not be metallic nor fabricated into any sort of planar structure since the bombarding flux is charge-neutralized. It is also possible to place different target materials adjacent to each other in the beam to make alloy structures that could not be fabricated into conventional diode targets.

K. Sputter deposition with alloys

Unlike evaporation, it is possible to sputter from a target which is composed of two or more species and deposit a film which is nominally similar composition to the target; with a few exceptions. Since the emission of atoms from a target is a kinetic, not a thermal, process, the vapor pressure of each constituent is irrelevant. And since most sputter targets are solid and kept well below the melting point, in most cases there can be no significant diffusion or flow within the target during the sputtering process which might rearrange the relative composition of the constituents during sputtering. Exceptions to this last case can be observed if there is significant ion-bombardment enhanced diffusion, which is driven by the compositional gradient in the near surface region due to the preferential sputtering of the higher yield component.[32] In a steady-state sputtering process, the emission rate of each of the constituents of an alloy must mirror the bulk composition, even though the sputter yield of each species may differ dramatically.

When an alloy target is sputtered for the first time, for a brief period of time the components of the alloy with the highest sputter yields are removed first. This reduces the surface composition of those components on the target, which effectively slows down the rate of removal of that higher yield species. The lower sputter yield components are enriched at the surface, and this leads to a relative increase in their emission rate. In the steady state situation, the surface composition of the target is altered such that the compositions of each component are scaled with the inverse of their relative sputter yield. This change in surface composition is known as an ''altered layer'' and extends a few atomic layers into the target.[33] The very first films deposited from a new alloy target will show this transition, and they will have proportionately higher levels of the higher sputter yield material than the bulk target. Once the steady state condition is reached, the sputter target is considered to be ''conditioned.''

This approach can be altered, though, due to a number of features. If, for example, the target contains a component such as oxygen or nitrogen which would normally be in the gas phase at the temperatures used, those atoms may not be included into the deposited film at the bulk composition due to losses of those species in the pumping system. In that case, it will be necessary to make up the loss by adding that species to the background gas. This is a version of reactive sputter deposition which will be discussed below. Second, if the emission profiles of each of the constituents of the alloy target are different; for example, if one component has an over-cosine distribution, the composition of the deposited films will vary spatially across the chamber. Finally, there may be energetic processes during the deposition, such as a sample bias voltage or the presence of negative ions from the cathode, which will result in bombardment of the film during deposition. Due to differences in the sputter yield, sample bombardment may result in removal of the higher yield components from the film. The latter effect is very common in cases of target materials with ionic bonding or with oxygen as one of its components. While probably present for most cases of oxide sputtering, this effect is most widely seen with the deposition of perovskite materials such as the yittrium–barium–copper–oxide superconductors.

L. Reactive sputter deposition

Much like the case of reactive evaporation, if a reactive gas species is present in the chamber during sputter deposition, it may be incorporated in both the films being deposited as well as the target material. The latter effect strongly impacts the nature of the deposition process and will have a measurable effect on film properties as well. The most straightforward case of reactive sputtering is to start with a pure, metallic target which is sputtered in an inert gas (such as Ar). Without any reactive gas species added, this would result in the deposition of metallic films of reasonable purity (assuming a good chamber base pressure, high purity Ar, etc.). If a reactive species is now added into the chamber, it may be incorporated into both the growing films on the sample and the chamber walls as well as the metallic target. The dynamics of this incorporation are shown in Figs. 10(a)–10(c), which plot the deposition rate, the chamber pressure, and the discharge voltage at constant applied power as a function of increasing reactive gas flow (and constant inert gas flow). This figure is most applicable to the case of reactive sputtering of a metal with oxygen. For the comparable case using nitrogen, Fig. 10(c) may increase at the transition point.

At the lowest reactive gas flows, the reactive species (oxygen, for example) is completely absorbed by the depositing films and the cathode surface. The film composition in this region would be very metallic but with oxygen levels well above the background levels. Surprisingly, the chamber pressure (or a mass spectrometer trace set to the gas species mass) shows no trace of the addition of the reactive species. The first reaction to this effect by many researchers is to recheck their flow controllers to see if there is even any gas flowing. The films and the cathode are functioning as efficient pumps for the reactive species.

As the flow of reactive gas is increased, the oxygen concentration in the films continues to increase. In addition, the cathode is beginning to oxidize, which results in a reduced sputter yield. In a practical sense, the erosion area of the cathode narrows slightly. Eventually, with even higher flow of the reactive species the cathode becomes covered with oxide. At this point, called the critical flow point, the sputtering rate of the cathode drops radically, and the emission of

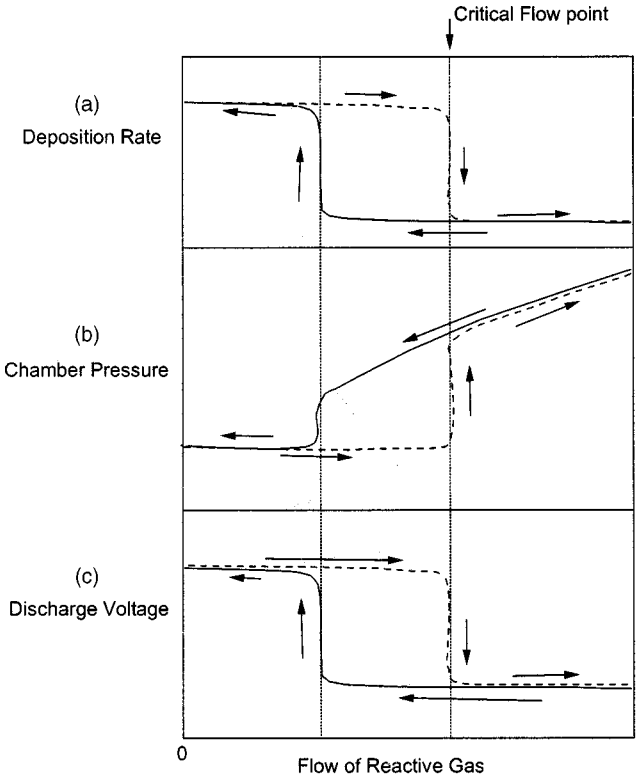

FIG. 10. Reactive sputter deposition transitions as a function of the flow of reactive gas.

the metallic species is slowed significantly. As the deposition rate of metal on the film surfaces drops, this reduces the pumping rate for the reactive gas species and this effectively increases the density of the reactive species in the chamber. The result is an irreversible transition to a completely reacted target with a very low sputter rate and a very low film deposition rate. At this point, however, the films are in their terminal oxide composition, which is the desired result. However, the deposition rate can be so low as to be almost unusable. An extreme example is the case of Al in oxygen, where the deposition rate drops 25× when the oxide transition is reached. If the reactive gas flow is reduced, the transition back to the metallic state is not reached until a much lower flow than the critical flow, due to the reduced sputter yield of the reacted, oxidized target compared to the metallic one. This is often characterized as a hysterisis curve due to the similarities to the magnetization of materials.

Much of the work in reactive sputter deposition over the past 20 years has focused on identifying, measuring, and then controlling this irreversible transition. The modeling work has been extensive, and is focused on the flow of atoms into and out of the chamber and various film surfaces.[34] On the experimental side, significant work and developments have been undertaken in the control of the reactive gas flow, such that deposition is undertaken at flows just below the critical flow but in a control mode which does not allow the complete cathode transition to take place.[35] An alternative to the flow control case is to use a pair of cathodes operated in a pulsed mode.

For the case of reactive deposition of oxides, it is usually sufficient simply to introduce oxygen into the deposition system: the oxidation reaction is sufficiently exothermic that the reaction occurs spontaneously at room temperature. For the equivalent nitride deposition case, however, the reactions often require energy to initiate, and this can take the form of drawing a bias current to the sample by biasing it negative of ground. A typical magnetron deposition system, with the dense plasma located close to the cathode, provides very little ion bombardment flux to a biased sample. A solution is called generically the ''unbalanced'' magnetron, and was first described by Windows.[36] In this device, the magnetic field near the cathode is designed such that additional magnetic field lines leave the vicinity of the cathode and impinge on the sample. Since electrons move easily along field lines, they move away from the cathode and set up a weak potential which draws ions from the magnetron cathode toward the sample. This allows a much higher bias current to be drawn to the sample, and this ion flux can be used to modify the chemical nature or structure of the depositing films.[37–39]

M. PVD film deposition and properties

The deposition and properties of the films made by any of the above-described PVD techniques depend strongly on a variety of parameters, such as the incident particle's energy and direction, the temperature and composition of the sample surface, any other energetic processes which might be occurring simultaneously (such as ion or electron bombardment), and chemistry. PVD techniques span a broad range in particle arrival energy, from nearly room temperature (0.05 eV) to many tens of electron volts. The directionality can vary from a single, fixed angle in a line-of-sight mode to a very wide angle, almost fog-like distribution. The temperature and composition of the sample surface have fairly little impact on the particle arrival process, but can strongly alter the residence time or mobility of the atoms on the surface, which can have an impact on film properties. Energetic ion, electron, or neutral bombardment of the film surface can alter the mobility of film atoms, resulting in changes in film structure or density.[40–42] At higher incident particle energy, film atoms may be resputtered from the film surface altogether. And finally, chemical reactions between the arriving film particles, the surface, and background gas atoms can change the composition of the deposited film, which, of course, may be intentional or unintended.

The energy present in any deposition process will strongly alter the properties of the deposited films. In an evaporative deposition, the arriving atoms at the film surface have a kinetic energy consistent with the temperature of the source they were emitted from. Typically, this would be 0.05 eV for a low temperature evaporation (<500 °C), up to 0.1–0.15 eV for the higher temperature evaporations. This kinetic energy has little effect on the deposition process. The arriving atoms in all PVD cases also bring along several electron volts of chemical or binding energy. This is essentially the energy of the bonds broken to remove the atom from the liquid phase at the source (or the solid phase in a sputtering process), and

this energy is deposited at the film surface upon condensation of the depositing atom. At low sample temperatures, evaporative depositions result in the low-speed impact of the arriving atom to the film surface and generally little mobility or motion afterwards. Structurally, this leads to a self-shadowing effect, which results in a columnar-like structure to the deposition. The resultant film has low density, large effective surface area, and is prone to absorption of moisture upon air exposure.

A depositing atom from a sputtering process brings along kinetic energy of typically a few electron volts and in some cases up to 20 eV or more. This is in addition to the above-mentioned chemical bond energy. The result of the additional kinetic energy is that the depositing atom can cause local rearrangement of the atoms at the film surface; a sort of atomic-scale short-term annealing process. This rearrangement results in less self-shadowing and a much denser film structure. While columnar microstructures can also be observed, the density is usually significantly closer to bulk density than with an evaporative deposition of the same material at the same temperature.

The directionality of the incoming atom can also alter the structure of the films deposited at low temperature. Evaporative depositions (including pulsed laser deposition and many arc deposition conditions) are almost always line-of-sight, in that the pressure is low enough that atoms emitted from the source travel to the sample without in-flight collisions with background gas atoms. The directionality aspect of evaporation exaggerates the columnar microstructure formation. However, in some applications, the directionality of the deposit is used for other purposes. For example, line-of-sight evaporative depositions allow the use of masks on or just above surfaces to delineate the deposition area. A widely used example of this is the photoresist technology used for semiconductor fabrication in the 1970s and early 1980s. A photosensitive polymer was configured on the surface such that after exposure, the sidewalls of the mask had slight overhangs. This allowed deposition adjacent to the photomask, but the sidewalls of the photoresist were not covered by the deposition. A subsequent solvent exposure then dissolved the photomask, and ''lifted off'' the unwanted film deposited on the mask area.

Another interesting application of the directional nature of evaporation is the formation of sculptured films which have controlled, but rather unusual structures.[43] An example is shown in Fig. 11. In this case, the sample surface was initially near-normal incidence to the deposition, but then was turned to a closer-to-grazing incidence. If the sample was then rotated slowly during deposition, the intrinsic self-shadowing effect results in a spiral or jagged form, based on the rate of turning of the sample.

Sputter deposition, by comparison, is almost always in a very nondirectional deposition configuration. This is caused by two effects; the increased gas pressure which leads to gas-phase scattering of the sputtered atoms, and second, by the extended area of most sputtering targets coupled with the short target-to-sample distance. The result is that sputter

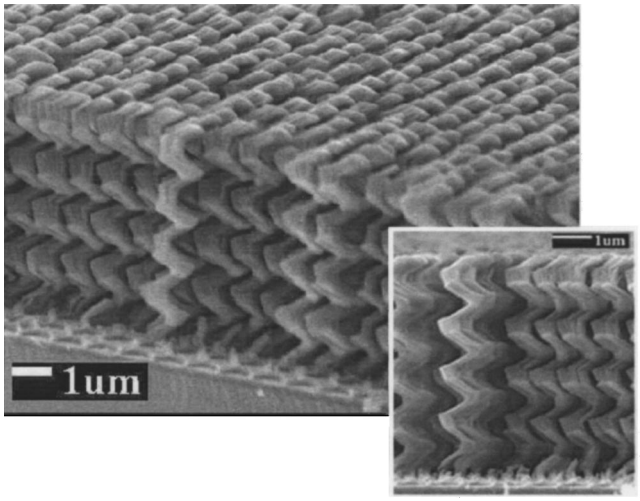

FIG. 11. A sculptured film deposited by glancing angle deposition (GLAD). Figure courtesy of M. Brett, University of Alberta (Ref. 39).

deposition of atoms results in arrival directions for the depositing atoms which range from near-normal incidence to grazing. One advantage of this wide distribution is the ability to make a continuous film over a step on the sample. This is the original use of the term ''step coverage'' and this was a significant advantage for the smoothing of surfaces and hermetic film coverage.

Conversely, sputter deposition can be carried out in a line-of-sight mode in certain circumstances. The most obvious is the case of ion beam deposition, where the pressure is low enough that in-flight gas collisions are rare. However, this is often compromised by the geometric configuration in most ion beam deposition tools which have a fairly short distance between the sputter target and the sample. If that distance is increased significantly (a few times the diameter of the ion beam), a line-of-sight deposition can be made, and this facilitates things like ''lift-off'' deposition using photoresist or contact masks. Generally, though, this is not widely done due to the low deposition rate for ion beam deposition which is then further reduced by the increased sample distance.

An alternative technique for increasing the directionality of a magnetron-based sputter deposition process is to use a geometric, spatial filter between the cathode and sample; the filter is called a collimator.[44] This filter is typically an array of tubes or holes with an aspect ratio (length of the tube/diameter) from 0.5 to 3. During the sputtering process, atoms which are moving with an angle far from normal incidence are likely to impact on the collimator walls and deposit there. Only atoms which are moving along the axis of the collimator tube will transit the collimator and make it to the sample. The degree of filtering is dependent on the collimator aspect ratio and can be easily calculated by simple ray-tracing from the target to the sample through the collimator. There is a significant effect on the net deposition rate, however. A collimator with an aspect ratio of 1:1 will have a 70% reduction in deposition rate compared to an open deposition system.

A more recent PVD alternative is to ionize some fraction of the sputtered atoms in flight and deposit a film from these

ions as well as the sputtered neutrals, a technique known as ionized PVD, or I-PVD.[45,46] The sputtered atoms can be ionized by the addition of a second plasma in the region between the cathode and sample. It is generally necessary to operate the system at higher pressure (15–25 mTorr) to have adequate metal ionization (30%–60%). At lower pressures, too many of the sputtered atoms transit the plasma without ionization. An alternative approach to I-PVD is to configure the magnetron cathode to cause some degree of ionization. Commercially, sources of this type have been developed in either a hollow cathode[47] or planar[48] geometry.

The principle application of directional PVD has been for semiconductor processing, particularly in the interconnect or wiring part of the wafer. The directional depositions are useful for depositing diffusion barriers and seed layers in trenches and vias. An I-PVD advantage (over collimated PVD) is that the ion energy can be increased by a sample bias such that the depositing metal ions may cause resputtering of the previously deposited film, leading to better sidewall coverage in deep features.

III. SUMMARY

This article has examined the PVD tools and techniques which are currently used to deposit and modify thin films. The characterization and applications of these films will be described in the following articles in this section. While the field of thin films may appear to be mature in that work has been under way since the 1800s, new studies and insight are continuing to be reported, and in many ways the field is posed to expand rapidly in the coming years. A great deal of the innovative work in PVD areas has been published, and will continue to be published in JVST.

Future directions in thin film technology will point both toward the atomic scale as well as in a completely different direction toward film deposition in solution. The former topic is driven by the relentless shrinkage in physical dimensions in semiconductor and related electronic devices. The latter topic is driven by the inherent difficulties in working either on a research scale or in practical, cost-competitive applications in ultrahigh vacuum. While film deposition in solution has been around for centuries in the form of electroplating, new techniques and tools are being developed to extend these and related technologies into the nanoscale range.

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EXHIBIT L

SILICON PROCESSING

FOR

THE VLSI ERA

VOLUME 2:

PROCESS INTEGRATION

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Published by:

Lattice Press,
Post Office Box 340
Sunset Beach, California 90742, U.S.A.

Cover design by Roy Montibon, Visionary Art Resources, Inc., Santa Ana, CA.

Library of Congress Cataloging in Publication Data
Wolf, Stanley

Silicon Processing for the VLSI Era
Volume 2 : Process Integration

Includes Index
1. Integrated circuits-Very large scale integration. 2. Silicon. I. Title

86- 81923

ISBN 0-961672-4-5

9 8 7 6 5 4 3 2

PRINTED IN THE UNITED STATES OF AMERICA

Oxygen is added to the CHF_3 gases being used to etch the oxide. The oxygen attacks the PR at a controlled rate, thereby producing lateral as well as vertical etching of the PR mask. More of the top SiO_2 is slowly exposed as vertical etching of the SiO_2 proceeds, and a sloped oxide sidewall is produced (Fig. 3-14b). Taper angles of 40-85° were obtained by varying the oxygen concentration.

Another technique for tapering contact-hole sidewalls without using resist erosion involves implantation of the surface of the oxide following deposition. This damages the top layer of the oxide and causes it to etch more rapidly, even when dry etching is used. The faster- etching top-surface layer causes a slope in the sidewalls.

A final group of processes utilizes two or more dry-etch steps to obtain tapered-sidewall profiles. In one example, a high-rate isotropic SiO_2 etch (i.e., with a lateral-to-vertical etch-rate ratio of 0.9 to 1 being exhibited for doped oxides) is used to etch the top portion of the contact-oxide layer, and an anisotropic-etch process is used to remove the oxide from the bottom of the contact hole.[26] In another, a downflow etcher operated at 2.45 GHz is used to etch part of a doped SiO_2 layer in an isotropic manner using a $CF_4 + O_2$ mixture; this is followed by an RIE step to give a vertical profile for the bottom portion of the layer.[27] A method that uses a tri-electrode dry-etch chamber for this type of process is described in reference 152 (Fig. 3-14c).

The problem of end-point detection for contact holes can also be difficult. That is, if a timed etch is used, a sufficient overetch must be allowed to ensure that all the contacts are opened. However, this demands a high selectivity to the Si to prevent too much Si from being consumed during the overetch. End-point detection is difficult, because the total area of the contacts being etched is significantly smaller compared to other layers. A technique for electronically enhancing the weak end-point signal produced when the contacts are finally opened is described in reference 144.

3.4.2.5 Removal of the Native-Oxide Layer Prior to Metal Deposition. Before the metal is deposited into the contact openings, it is necessary to ensure that the exposed silicon surface is as free as possible of contamination or of a native-oxide layer. Silicon will grow a thin native oxide within a matter of seconds upon exposure to an oxygen-containing ambient or an oxidizing solution. This native oxide can represent an impediment to current flow through the contact interface, result-

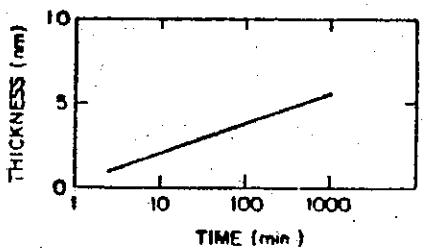

Fig. 3-15 Native oxide growth rate on Si exposed to room air.[28] Copyright 1984. Reprinted with permission of the AIOP.

ing in high resistance for ohmic contacts. Oxide films of minimum thickness (2–5Å) do not present a problem, since many contact metals (e.g., Al, Ti, Pt) can consume such thin oxide layers during the sinter step. Nevertheless, as shown in Fig. 3-15, the native-oxide layer can grow thicker than this value in 30 to 60 minutes* if the Si is exposed to atmosphere at room temperature.[28,139] Consequently, techniques must normally be employed to remove native oxide layers on Si, and the metal must be deposited quickly enough after such premetal cleaning that the film does not have enough time to regrow.

A variety of techniques have been suggested for cleaning the Si prior to metal deposition. Polymers deposited during a dry-etch step used to etch the contact oxide are typically removed through a final oxygen-ashing step. This step may, however, may create a thin oxide layer on the exposed Si. The most widely used method for removing native-oxide layers on the Si involves dipping the wafer in a dilute H_2O:HF (100:1) solution for ~1 minute, followed by rinsing and drying and immediate insertion into the sputter or evaporation chamber. (The HF dip also serves to remove heavy-metal contamination that might occur as a result of the dry-etch process.)

It is acknowledged that this method is not perfect, since some SiO_2 will regrow on the Si during the rinse-and-dry step, and inadequate wetting may prevent complete removal of the native oxide in small-geometry contacts. Therefore, a technique of sputter-etching the contacts in the sputter chamber and depositing the metal before reexposing the contacts to atmospheric conditions is also frequently used in addition to the HF dip. Most sputtering systems currently provide the capability for performing such sputter etching.

However, some concerns have also been raised about sputter etching. For small, high-aspect-ratio contact holes, sputtering and redeposition of material from the contact sidewalls and the wafer surface may cause more oxide to be deposited onto the Si than is removed through the sputter-etch process (Fig. 3-16).[29] Two alternative procedures to overcome these concerns have therefore been suggested. The first involves an in situ, chemically driven dry-etch step to remove the native oxide. While this would eliminate the resputtering effect, it would require that sputtering equipment be designed with this extra capability; no such products have yet been commercially introduced. In the second approach, an anhydrous-HF gas could be used to remove the native oxide, as described in a previous section.

The effect of "dirty" Si surfaces prior to Al deposition has been studied by Faith et al.[30] These researchers showed that if the Si surface is not successfully cleaned prior to Al deposition, the post-sinter contact resistance will be an order of magnitude higher than if an effective pre-metal clean had been used. They also noted that clean contacts

*A recent report indicates that both moisture and oxygen must be present in air in order for the oxide to grow. Furthermore, if oxygen is present in DI water, a native oxide will also grow when Si wafers are immersed in it. Since the growth rate of native oxide decreases with the concentration of moisture, this may provide an approach to the control of native-oxide films on Si.[147] For example, virtually no native oxide was observed to grow during a seven day period of time when Si wafers were stored in air containing < 0.1 ppm moisture.

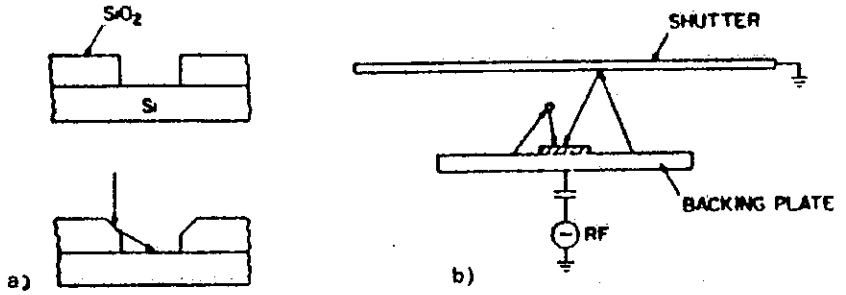

Fig. 3-16 Sources of contamination of Si surface at the bottom of the contact hole as a result of RIE. (a) Faceting occurs during anisotropic etching of contact openings. Material sputtered from the facet deposits in the contact opening at a rate that may exceed the rate of removal of the material from the bottom of the opening. (b) Backscattering of material sputtered from the backing plate may occur due to collisions with gas molecules of the glow discharge or from reflection from the shutter.[28] Copyright 1984. Reprinted with permission of the AIOP.

exhibit a lower contact resistance than dirty ones *prior* to the sinter step, and that this effect could be exploited to test the contacts prior to sintering. If a dirty interface were detected at that point, a decision to strip and rework the metal might still be possible, whereas this option would no longer be available once sintering had been performed. As described in the following section on contact sintering, ion-beam mixing has also been proposed as a way to disperse any native-oxide layers at the interface.

3.4.2.6 Metal Deposition and Patterning. The major issue in the deposition of metal for fabricating contacts is ensuring that adequate step coverage is obtained into the contact holes. When contact-hole sizes are comparable to the oxide thickness (i.e., when the holes have high aspect ratios), good step coverage can be difficult to achieve. The deposition process, as well as the profile of the contact-hole sidewalls, can significantly impact the quality of the step coverage. Several aspects of the metal- deposition procedure can also play a role in this issue.

First, the type of process selected for deposition is significant. Some CVD processes can completely fill high-aspect-ratio contact holes, even those with nearly vertical sidewalls, while physical vapor deposition (PVD) methods are not apt to fill the holes so well. This advantage has been exploited in filling contact holes with CVD W (selectively and through blanket deposition). Polysilicon and selectively grown epitaxial layers of Si are other CVD processes that have been reported for such contact-filling applications.

If films are needed that cannot be deposited by CVD, the conditions of the PVD process can be selected to give improved step coverage (see chap. 4 in this volume, and Vol. 1, chap. 10). For example, heating of the wafers to ~300-350°C has been shown to significantly improve the step coverage of sputtered Al films into contact holes. Full planarization (i.e., complete filling of the holes) has also been demonstrated by applying

EXHIBIT 29

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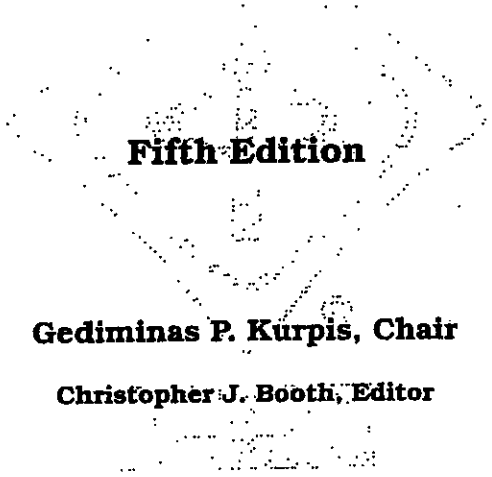

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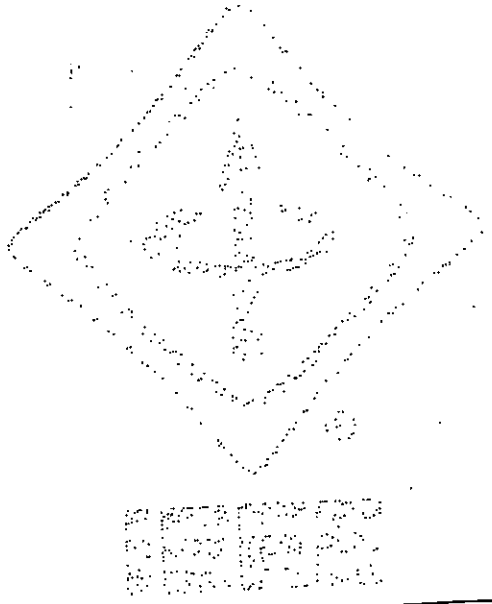

The Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street, New York, NY 10017-2394, USA

ISBN 1-55937-240-0

SH15594

January 15, 1993

gon autotransformer," or a "squashed delta." C57.12.80-1978

interconnected star connection of polyphase circuits. *See:* **zig-zag connection of polyphase circuits.**

interconnected system (electric power systems). A system consisting of two or more individual power systems normally operating with connecting tie lines. *See:* **power system.** 94-1970w, [54]

interconnected system. Two or more power systems connected by transmission facilities. 94-1991

interconnecting channel (of a supervisory system) (power switchgear). The transmission link, such as the direct wire, carrier, or microwave channel (including the direct current, tones, etc.) by which supervisory control or indication signals or selected telemeter readings are transmitted between the master station and the remote station or stations, in a single supervisory system. C37.100-1981

interconnection. The physical plant and equipment required to facilitate the transfer of electric energy between two or more entities. It can consist of a substation and an associated transmission line and communications facilities or only a simple electric power feeder. 1109-1990

interconnection device. *See:* **adapter.**

interconnection diagram (packaging machinery). A diagram showing the connections between the terminals in the control panel and outside points, such as connections to motors and auxiliary devices. 333-1980w

interconnection tie. A feeder interconnecting two electric supply systems. *Note:* The normal flow of energy in such a feeder may be in either direction. *See:* **center of distribution.** [10]

interconnect space. The address space used for board identification, system configuration, and board specific functions such as testing and diagnostics. 1296-1987

interconnect template. A definition of the contents of the interconnect space of an agent. 1296-1987

interdendritic corrosion. Corrosive attack that progresses preferentially along interdendritic paths. *Note:* This type of attack results from local differences in composition, that is, coring, commonly encountered in alloy castings. [59]

interdigital magnetron. A magnetron having axial anode segments around the cathode, alternate segments being connected together at one end, remaining segments connected together at the opposite end. 161-1971w, [45]

interdigit interval (telephony) (dial-pulse address signaling systems). In dial-pulse signaling, an extended make interval used to separate and distinguish successive dial-pulse address digits. 753-1983w

interdigit (interdigital) time (measuring the performance of tone address signaling systems). The time interval between successive signal present intervals during which no signal present condition exists. This time includes the signal off condition and transition intervals between signal off condition and signal present condition on both state transitions. 752-1986

interelectrode capacitance (*j-I* interelectrode capacitance C_{jI} of an *n*-terminal electrode tube). The capacitance determined from the short-circuit transfer admittance between the *j*th and the *I*th terminals. *Note:* This quantity is often referred to as direct interelectrode capacitance. *See:* **electron-tube admittance.** 161-1971w

interelectrode transadmittance (*j-I* interelectrode transadmittance of an *n*-electrode electron tube). The short-circuit transfer admittance from the *j*th electrode to the *I*th electrode. *See:* **electron-tube admittances.** 161-1971w

interelectrode transconductance (*j-I* interelectrode transconductance). The real part of the *j-I* interelectrode transadmittance. *See:* **electron-tube admittances.** 161-1971w

interelement influences (polyphase wattmeters). The percentage change in the recorded value that is caused solely by the action of the stray field of one element upon the other element. *Note:* This influence is determined at the specified frequency of calibration with rated current and rated voltage in phase on both elements or such lesser value of equal currents in both elements as gives end-scale deflection. Both current and voltage in one element shall then be reversed, and, for rating purposes, one-half the difference in the readings in percent is the interelement influence. *See:* **accuracy rating (instrument).** [102], [111]

interface (general-system term) (1) (696 interface devices). A shared electrical boundary between parts of a computer system, through which information is conveyed. 696-1983
(general system terms) (2) (microcomputer system bus). A shared boundary between two systems, or between parts of systems, through which information is conveyed. 796-1983
(3) (microprocessor operating systems). A shared boundary between two layers or modules of software. 855-1985
(4) (watthour meters). The means for transmitting information between the register and peripheral equipment. C12.13-1985
(5) (general). A shared boundary. [20], [85]
(6) (nuclear power generating stations) (class 1E equipment). A junction or junctions between a Class 1E equipment and another equipment or device. (Examples: connection boxes, splices, terminal boards, electrical con-